UCC28180 可编程频率、连续导通模式 (CCM)、升压功率因数校正 (PFC) 控制器

1 特性

- 8 引脚解决方案（无需 AC 线路感测）
- 宽范围可编程开关频率（对于基于金属氧化物半导体场效应晶体管 (MOSFET) 和基于绝缘栅双极型晶体管 (IGBT) 的 PFC 控制器为 18kHz 至 250kHz）
- 用于降低 iTHD 的经调整电流环路
- 电流感测阈值有所降低（最大限度降低分流电阻功耗）
- 平均电流模式控制
- 软过流和逐周期峰值电流限制保护
- 具有滞后恢复功能的输出过压保护
- 可闻噪声最小化电路
- 开环检测
- 改善输出过压和欠压状态期间的动态响应
- 最高占空比为 96%（典型值）
- 针对无负载稳压的突发模式
- VCC 欠压锁定 (UVLO)、低附加动态功耗电流 (ICC) 启动 (< 75μA)

2 应用

- 100 瓦到几千瓦范围内的通用交流输入、CCM 升压 PFC 转换器
- 服务器和台式机电源
- 大型家用电器（空调、冰箱）
- 工业电源（德国标准化学会 (DIN) 电源轨）
- 平板（等离子 (PDP)、液晶 (LCD) 和发光二级管 (LED)）电视

3 说明

UCC28180 是一款灵活且易于使用的 8 引脚有源功率因数校正 (PFC) 控制器，该控制器运行在连续导通模式 (CCM) 下，可为交流-直流前端中的升压前置稳压器提供高功率因数、低电流失真和出色的电压稳压。此控制器适用于 100 瓦至几千瓦范围内的通用交流输入系统，开关频率可在 18kHz 至 250kHz 范围内编程，以便轻松支持功率 MOSFET 和 IGBT 开关。集成的 1.5A 和 2A (SRC-SNK) 峰值栅极驱动输出在内部钳位为 15.2V（典型值），无需使用缓冲电路即可快速接通、关闭以及轻松管理外部电源开关。

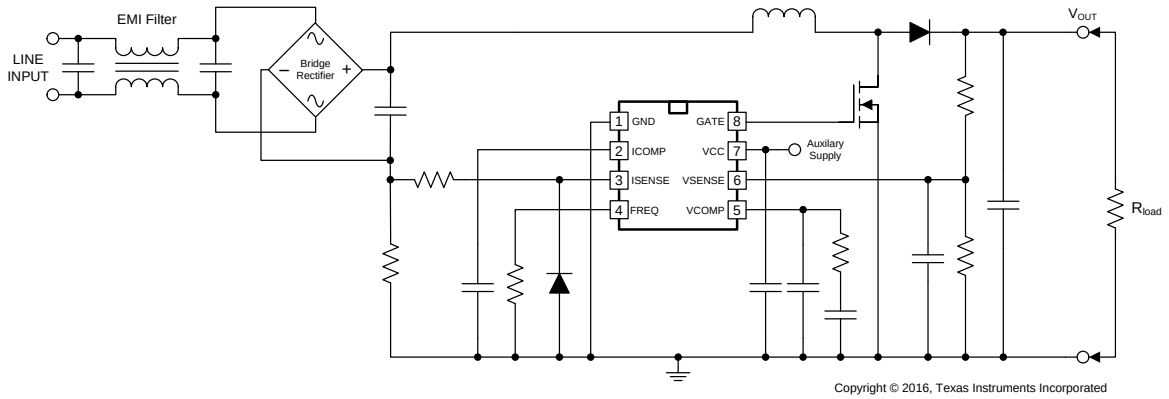
通过使用平均电流模式控制，在无需输入线路感测的情况下，即可实现输入电流低失真波整形，从而减少了外部组件数量。此外，该控制器 的 电流感测阈值有所降低，方便使用低值分流电阻来降低功率耗散，这对于高功率系统尤为重要。为了实现低电流失真，此控制器还特有 用于消除相关误差的经调整电流环路稳压电路。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
UCC28180	SOIC (8)	4.90mm x 3.91mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用电路原理图



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4 修订历史记录

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- 已更改 C 版本历史记录中的页码，更正了关于功能框图中增加的二极管的页码。 ... 2
- 已更改 text value of 0.538 to 0.366 to align with 公式 85. Updated change was implemented in the C revision and recorded in the D revision. ... 31
- 已添加 D4 to 表 2. Updated change was implemented in the C revision and recorded in the D revision. ... 37
- 已添加 接收文档更新通知. ... 39
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- 已添加 一个二极管至典型应用原理图。 ... 1
- 已更改 ICC Standby current MAX rate from 2.95 mA to 3.47 mA. ... 6
- 已更改 ISENSE threshold, soft over current (SOC) TYP value from –0.295 V to –0.285 V. ... 6
- 已更改 Maximum current under EDR operation MAX rating from –241 µA to –275 µA. ... 6
- 已添加 a diode to the Functional Block Diagram. ... 13
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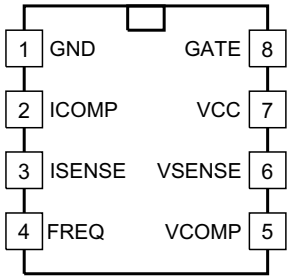
- 已添加 *ESD 额定值表*，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分和*机械、封装与可订购信息*部分 ... 1

5 说明 （续）

简单外部网络可实现电流和电压控制环路的灵活补偿。此外，UCC28180 提供一个基于电压反馈信号的增强型动态响应电路，此电路可改善在过压和欠压情况下对快速负载瞬变的响应。UCC28180 内提供的独特 VCOMP 放电电路会在电压反馈信号超过 V_{OVP_L} 时激活，从而使控制环路能够快速稳定下来并避免触发过压保护功能。触发过压保护功能时，脉宽调制 (PWM) 的关闭经常会引起可闻噪声。受控软启动在启动期间逐渐调节输入电流，并减小电源开关上的应力。此控制器提供多种系统级 保护 ，其中包括 VCC UVLO、峰值电流限制、软过流保护、输出开环检测，输出过压保护和引脚开路检测 (VISNS)。经调整的内部基准提供精确保护阈值和稳压设定值。用户可通过将 VSENSE 引脚下拉至低于 0.82V 来控制低功耗待机模式。

6 Pin Configuration and Functions

8-Pin SOIC
D Package
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GATE	8	O	**Gate Drive:** Integrated push-pull gate driver for one or more external power MOSFETs. Typical 2.0-A sink and 1.5-A source capability. Output voltage is typically clamped at 15.2 V (typical).
GND	1		**Ground:** device ground reference.
ICOMP	2	O	**Current Loop Compensation:** Transconductance current amplifier output. A capacitor connected to GND provides compensation and averaging of the current sense signal in the current control loop. The controller is disabled if the voltage on ICOMP is less than 0.2 V, (ICOMPP protection function).
ISENSE	3	I	**Inductor Current Sense:** Input for the voltage across the external current sense resistor, which represents the instantaneous current through the PFC boost inductor. This voltage is averaged by the current amplifier to eliminate the effects of ripple and noise. *Soft Over Current (SOC)* limits the average inductor current. *Cycle-by-cycle peak current limit (PCL)* immediately shuts off the GATE drive if the peak-limit voltage is exceeded. An internal 2.3-µA current source pulls ISENSE above 0.085 V to shut down PFC operation if this pin becomes open-circuited, (ISOP protection function). Use a 220-Ω resistor between this pin and the current sense resistor to limit inrush-surge currents into this pin.
VCC	7		**Device Supply:** External bias supply input. *Under-Voltage Lockout (UVLO)* disables the controller until VCC exceeds a turn-on threshold of 11.5 V. Operation continues until VCC falls below the turn-off (UVLO) threshold of 9.5 V. A ceramic by-pass capacitor of 0.1 µF minimum value should be connected from VCC to GND as close to the device as possible for high-frequency filtering of the VCC voltage.
VCOMP	5	O	**Voltage Loop Compensation:** Transconductance voltage error amplifier output. A resistor-capacitor network connected from this pin to GND provides compensation. VCOMP is held at GND until VCC, and VSENSE exceed their threshold voltages. Once these conditions are satisfied, VCOMP is charged until the VSENSE voltage reaches its nominal regulation level. When Enhanced Dynamic Response (EDR) is engaged, a higher transconductance is applied to VCOMP to reduce the charge or discharge time for faster transient response. *Soft Start* is programmed by the capacitance on this pin. VCOMP is pulled low when VCC UVLO, OLP/Standby, ICOMPP and ISOP functions are activated.
FREQ	4	O	**Switching Frequency Setting:** This pin allows the setting of the operating switching frequency by connecting a resistor to ground. The programmable frequency range is from 18 kHz to 250 kHz.
VSENSE	6	I	**Output Voltage Sense:** An external resistor-divider network connected from this pin to the PFC output voltage provides feedback sensing for regulation to the internal 5-V reference voltage. A small capacitor from this pin to GND filters high-frequency noise. Standby disables the controller and discharges VCOMP when the voltage at VSENSE drops below the Open-Loop Protection (OLP) threshold of 16.5%V_{REF} (0.82 V). An internal 100-nA current source pulls VSENSE to GND during pin disconnection. *Enhanced Dynamic Response (EDR)* rapidly returns the output voltage to its normal regulation level when a system line or load step causes VSENSE to rise above 105% or fall below 95% of the reference voltage. Two level *Output Over-Voltage Protection (OVP):* a 4-kΩ resistor connects VCOMP to ground to rapidly discharge VCOMP when VSENSE exceeds 107% (V_{OVP_L}) of the reference voltage. If VSENSE exceeds 109% (V_{OVP_H}) of the reference voltage, GATE output will be disabled until VSENSE drops below 102% of the reference voltage.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, all voltages are with respect to GND (unless otherwise noted). Currents are positive into and negative out of the specified terminal.

		MIN	MAX	UNIT
Input voltage range	VCC, GATE	–0.3	22	V
	FREQ, VSENSE, VCOMP, ICOMP	–0.3	7	
	ISENSE	–24	7	
Input current range	VSENSE, ISENSE	–1	1	mA
Junction temperature, T_J	Operating	–55	150	°C
Lead temperature, T_{SOL}	Soldering, 10 s		300	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	VCC_{OFF} + 1V	21	V
Operating junction temperature, T_J	–40	125	°C
Operating frequency	18	250	kHz

7.4 Thermal Information

THERMAL METRIC(1)		UCC28180 D 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	116.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance(3)	62.2	
$R_{\theta JB}$	Junction-to-board thermal resistance(4)	56.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.4	
ψ_{JB}	Junction-to-board characterization parameter(6)	55.9	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).

7.5 Electrical Characteristics

Unless otherwise noted, VCC=15Vdc, 0.1µF from VCC to GND, –40°C ≤ T_J = T_A ≤ +125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
$ICC_{PRESTART}$	ICC Pre-start current	VCC = VCC_{OFF} – 0.2 V			75	µA
ICC_{STBY}	ICC Standby current	VSENSE = 0.5 V	1.8	2.4	3.47	mA
ICC_{ON_load}	ICC Operating current	VSENSE = 4.0 V, C_{GATE} = 4.7 nF	5.8	7	8.8	mA
UNDER VOLTAGE LOCKOUT (UVLO)						
VCC_{ON}	VCC Turn on threshold		10.8	11.5	12.1	V
VCC_{OFF}	VCC Turn off threshold		9.1	9.5	10.3	V
	UVLO Hysteresis		1.6	1.7	2	V
VARIABLE FREQUENCY						
f_{SW}	Minimum switching frequency	R_{FREQ} = 130 kΩ	16.3	18	19.8	kHz
	Typical switching frequency	R_{FREQ} = 32.7 kΩ	61.75	65	68.25	kHz
	Maximum switching frequency	R_{FREQ} = 8.2 kΩ	225	250	275	kHz
V_{FREQ}	Voltage at FREQ pin	T_A = 25°C	1.43	1.5	1.56	V
PWM						
D_{MIN}	Minimum duty cycle	VSENSE = 5.1 V, ISENSE = –0.25 V			0%	
D_{MAX}	Maximum duty cycle	VSENSE = 4.0 V, R_{FREQ} = 32.7 Ω	94.8%	96.5%	98%	
$t_{OFF(min)}$	Minimum off time	VSENSE = 3 V, I_{COMP} = 0.72 V	450	570	690	ns
SYSTEM PROTECTION						
V_{SOC}	ISENSE threshold, soft over current (SOC)		–0.259	–0.285	–0.312	V
V_{PCL}	ISENSE threshold, peak current limit (PCL)		–0.345	–0.4	–0.438	V
I_{ISOP}	ISENSE bias current, ISENSE open-pin protection (ISOP)	ISENSE = 0 V		–2.3	–2.95	µA
V_{ISOP}	ISENSE threshold, ISENSE open-pin protection (ISOP)	ISENSE = open pin		0.085	0.14	V
V_{OLP}	VSENSE threshold, open loop protection (OLP)	ICOMP = 1 V, ISENSE = 0 V	15.6	16.5	17.6	$\%V_{REF}$
	Open loop protection (OLP) Internal pull-down current	VSENSE = 0.5 V		100	325	nA
V_{UVD}	VSENSE threshold, output under-voltage detection (UVD) used for enhanced dynamic response(1)		93.25	95	97	$\%V_{REF}$
V_{OVD}	VSENSE threshold, output over-voltage detection (OVD) used for Enhanced dynamic response(1)		103	105	106.75	$\%V_{REF}$
V_{OVP_L}	Output over-voltage protection low threshold, VCOMP is discharged by a 4kΩ resistor when VSENSE > V_{OVP_L}		105	107	109	$\%V_{REF}$
V_{OVP_H}	Output over-voltage protection high threshold, PWM shuts off when VSENSE > V_{OVP_H}		107	109	111	$\%V_{REF}$
$V_{OVP\_H(RST)}$	Output over-voltage protection (VOVP_H) reset threshold, PWM turns on when VSENSE < $V_{OVP\_H(RST)}$		100	102	104	$\%V_{REF}$
	ICOMP threshold, external overload protection			0.2	0.25	$\%V_{REF}$
CURRENT LOOP						
g_{mi}	Transconductance gain		0.75	0.95	1.1	mS
	Output linear range (1)			±50		µA
	ICOMP voltage during OLP	VSENSE = 0 V	2.7	3	3.3	V
VOLTAGE LOOP						
V_{REF}	Reference voltage	T_A = 25°C	4.93	5	5.07	V
		–40°C ≤ T_A ≤ +125°C	4.87	5	5.15	V
g_{mv}	Transconductance gain without EDR		–40	–56	–70	µS
$g_{mv\text{-}EDR}$	Transconductance gain under EDR		–230	–280	–340	µS
	Maximum sink current under normal operation	VSENSE = 5 V, VCOMP = 4 V	23	40	57	µA
	Source current under soft start	VSENSE = 4 V, VCOMP = 4 V	–29	–40	–52	µA
	Maximum current under EDR operation	VSENSE = 4 V, VCOMP = 2.5 V		–200	–275	µA

(1) Not production tested. Characterized by design

Electrical Characteristics (接下页)

Unless otherwise noted, VCC=15Vdc, 0.1µF from VCC to GND, –40°C ≤ T_J = T_A ≤ +125°C. All voltages are with respect to GND. Currents are positive into and negative out of the specified terminal.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	VSENSE input bias current	VSENSE = 5 V	20	100	250	nA
	VCOMP voltage during OLP	VSENSE = 0.5 V, I_{VCOMP}= 0.5 mA	0	0.04	0.10	V
	VCOMP rapid discharge current	VCOMP = 2 V, VCC = floating		0.37		mA
$V_{PRECHARGE}$	VCOMP precharge voltage	I_{VCOMP} = –100 µA, VSENSE = 4 V		1.5		V
$I_{PRECHARGE}$	VCOMP precharge current	VCOMP = 0 V		–1		mA
	VSENSE threshold, end-of-soft-start	Initial Start-up		98		%V_{REF}
GATE DRIVER						
	GATE current, peak, sinking(1)	C_{GATE} = 4.7 nF		2		A
	GATE current, peak, sourcing(1)	C_{GATE} = 4.7 nF		–1.5		A
	GATE rise time	C_{GATE} = 4.7 nF, GATE = 2 V to 8 V	8	40	60	ns
	GATE fall time	C_{GATE} = 4.7 nF, GATE = 8 V to 2 V	8	25	40	ns
	GATE low voltage, no load	I_{GATE} = 0 A		0	0.01	V
	GATE low voltage, sinking	I_{GATE} = 20 mA		0.04	0.06	V
	GATE low voltage, sourcing	I_{GATE} = -20 mA		–0.04	–0.06	V
	GATE low voltage, sinking, OFF	VCC = 5 V, I_{GATE} = 5 mA	0.1	0.2	0.31	V
	GATE low voltage, sinking, OFF	VCC = 5 V, I_{GATE} = 20 mA	0.4	0.8	1.4	V
	GATE high voltage	VCC = 20 V, C_{GATE} = 4.7 nF	14.5	15.2	16.1	V
	GATE high voltage	VCC = 12.2 V, C_{GATE} = 4.7 nF	10.8	11.2	12	V
	GATE high voltage	VCC = VCC_{OFF} + 0.2 V, C_{GATE} = 4.7 nF	8.2	9	10.1	V

7.6 Typical Characteristics

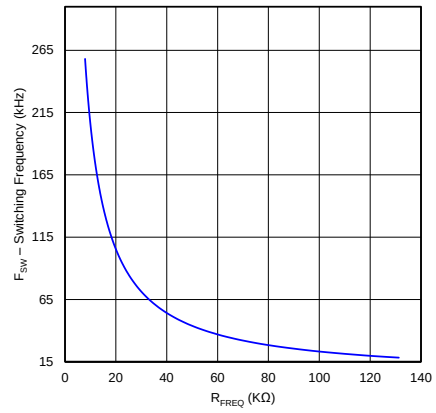
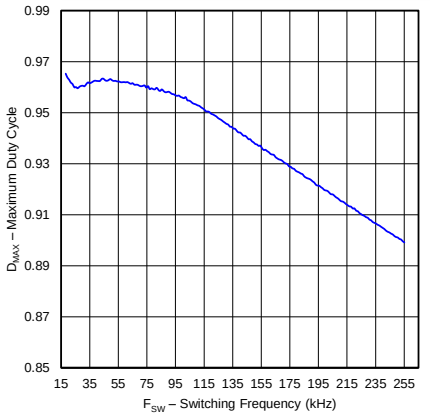


图 1. Switching Frequency vs. Resistor



VCC = 15 V

图 2. Maximum Duty Cycle vs. Switching Frequency

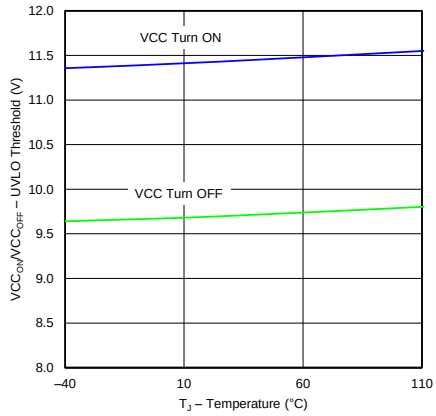
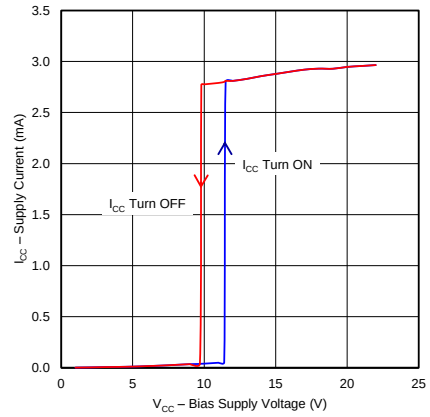
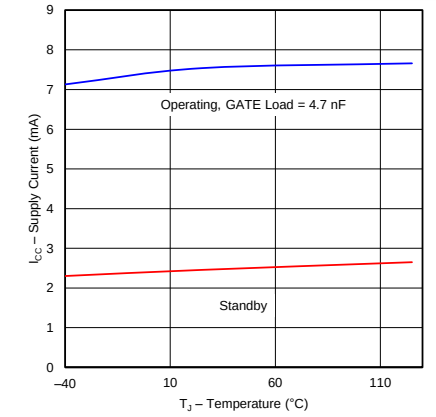


图 3. UVLO Threshold vs. Temperature



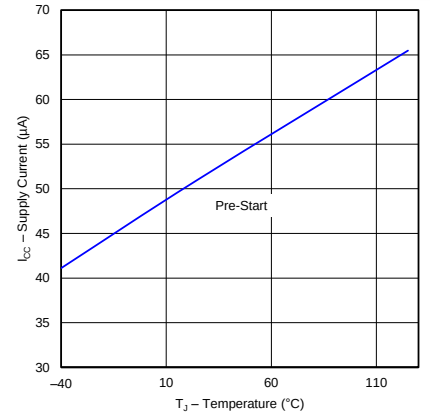
T_J = 25 °C VSENSE= 3 V
No Gate Load F_{SW} = 65 kHz

图 4. Supply Current vs. Bias Supply Voltage



VCC = 15 V

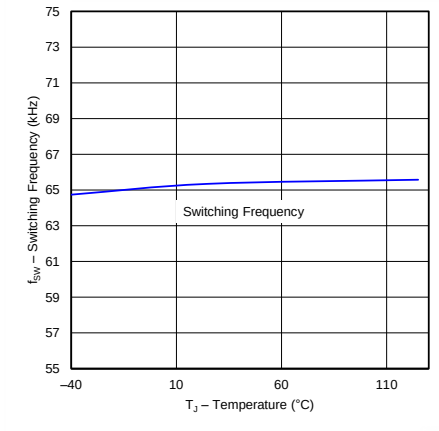
图 5. Supply Current vs. Temperature



VCC = VCC_{ON} – 0.2 V

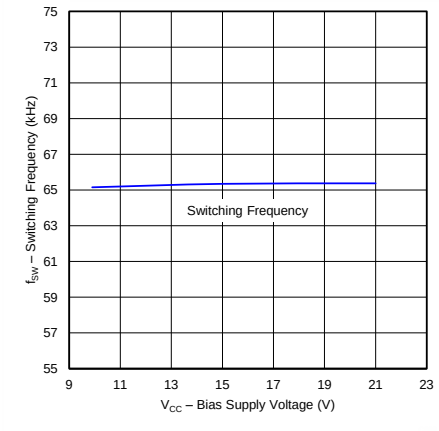
图 6. Pre-Start Supply Current vs. Temperature

Typical Characteristics (接下页)



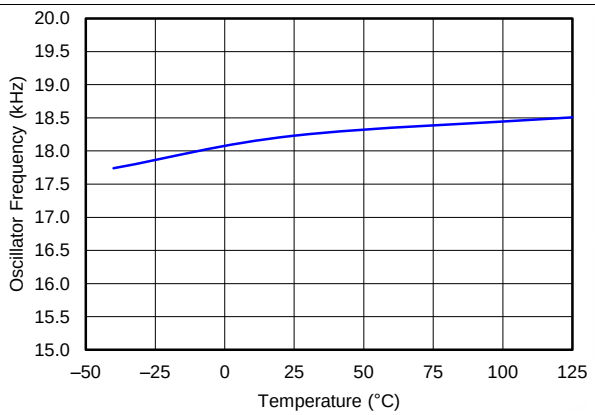
VCC = 15 V F_{SW} = 65 kHz

图 7. Oscillator Frequency (65 kHz) vs. Temperature



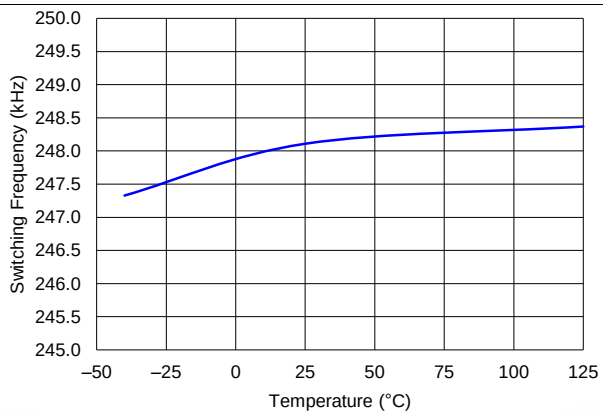
T_J = 25 °C F_{SW} = 65 kHz

图 8. Oscillator Frequency (65 kHz) vs. Bias Supply Voltage



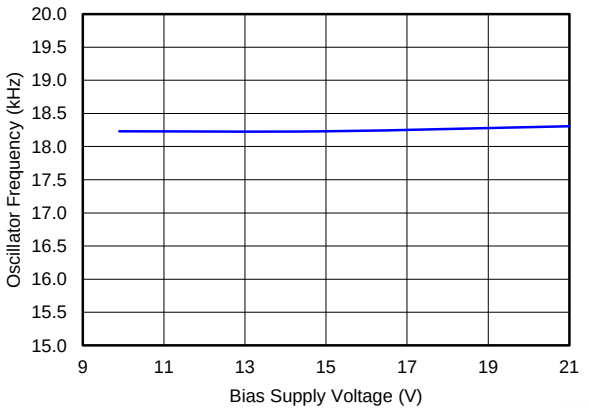
VCC = 15 V

图 9. Oscillator Frequency (18 kHz) vs. Temperature



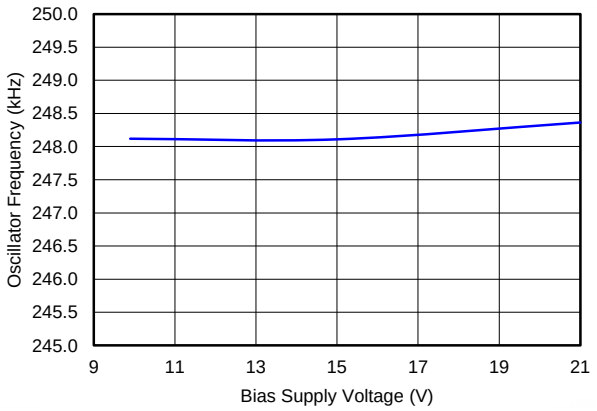
VCC = 15 V

图 10. Oscillator Frequency (250 kHz) vs. Temperature



T_J = 25 °C

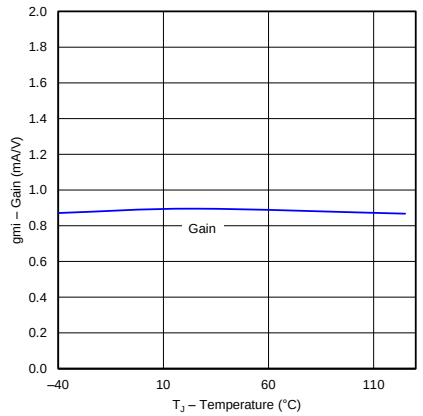
图 11. Oscillator Frequency (18 kHz) vs. Bias Voltage



T_J = 25 °C

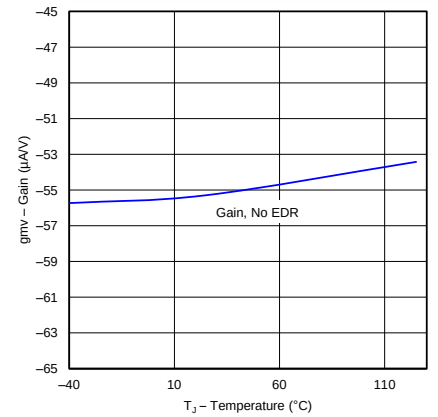
图 12. Oscillator Frequency (250 kHz) vs. Bias Voltage

Typical Characteristics (接下页)



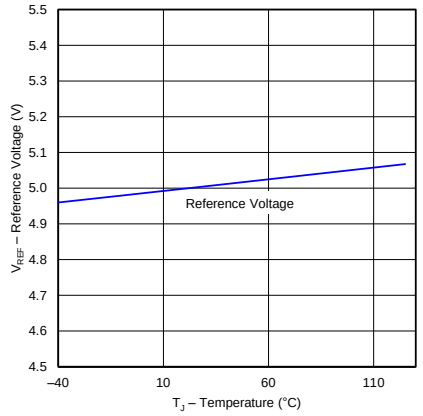
VCC = 15 V

图 13. Current Loop Gain vs. Temperature



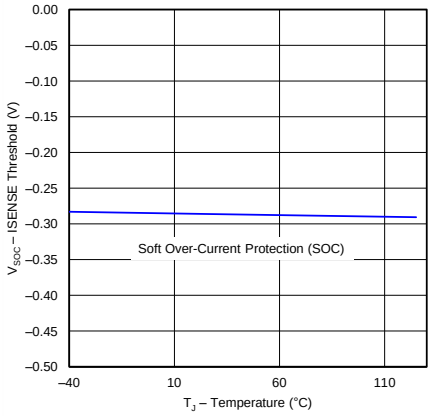
VCC = 15 V

图 14. Voltage Loop Gain vs. Temperature



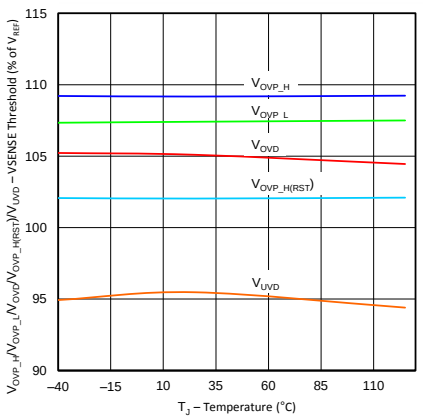
VCC = 15 V

图 15. Reference Voltage vs. Temperature



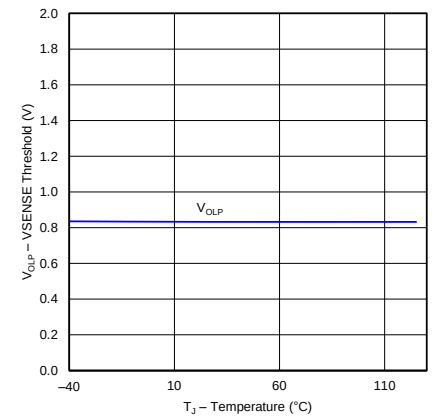
VCC = 15 V

图 16. I_{SENSE} Threshold Soft Over Current (SOC) vs. Temperature



VCC = 15 V

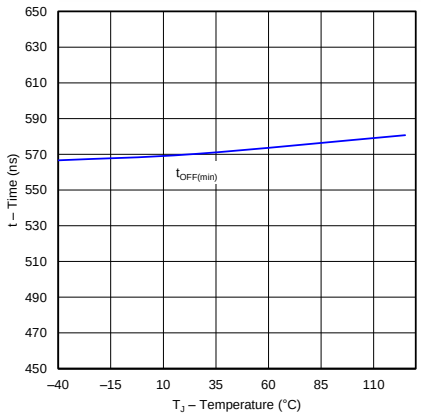
图 17. VSENSE Threshold vs. Temperature



VCC = 15 V

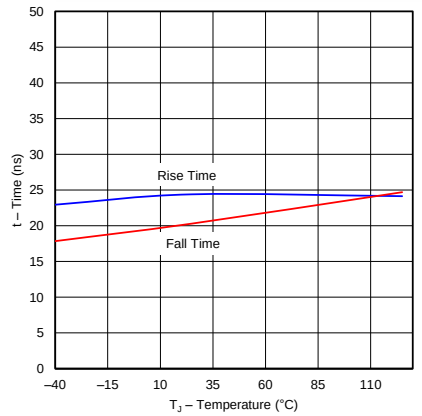
图 18. VSENSE Threshold Open Loop vs. Temperature

Typical Characteristics (接下页)



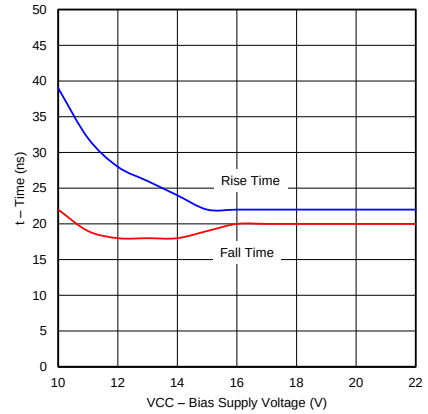
ICOMP = 0.72 V VSENSE = 3 V F_{SW} = 65 kHz

图 19. Minimum Off Time vs. Temperature



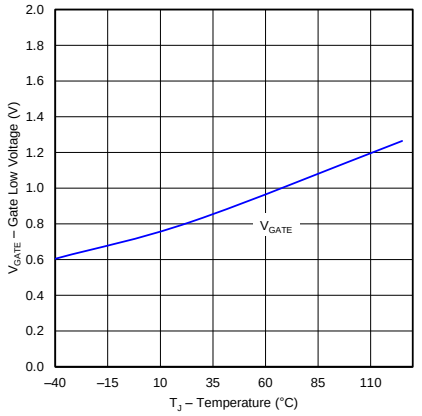
VCC = 15 V C_{GATE} = 4.7 nF V_{GATE} = 2 V-8 V

图 20. Gate Drive Rise/Fall Time vs. Temperature



T_J = 25 °C C_{GATE} = 4.7 nF V_{GATE} = 2 V-8 V

图 21. Gate Drive Rise/Fall Time vs. Bias Supply Voltage



VCC = 15 V I_{GATE} = 20 mA

图 22. Gate Low Voltage vs. Temperature

8 Detailed Description

8.1 Overview

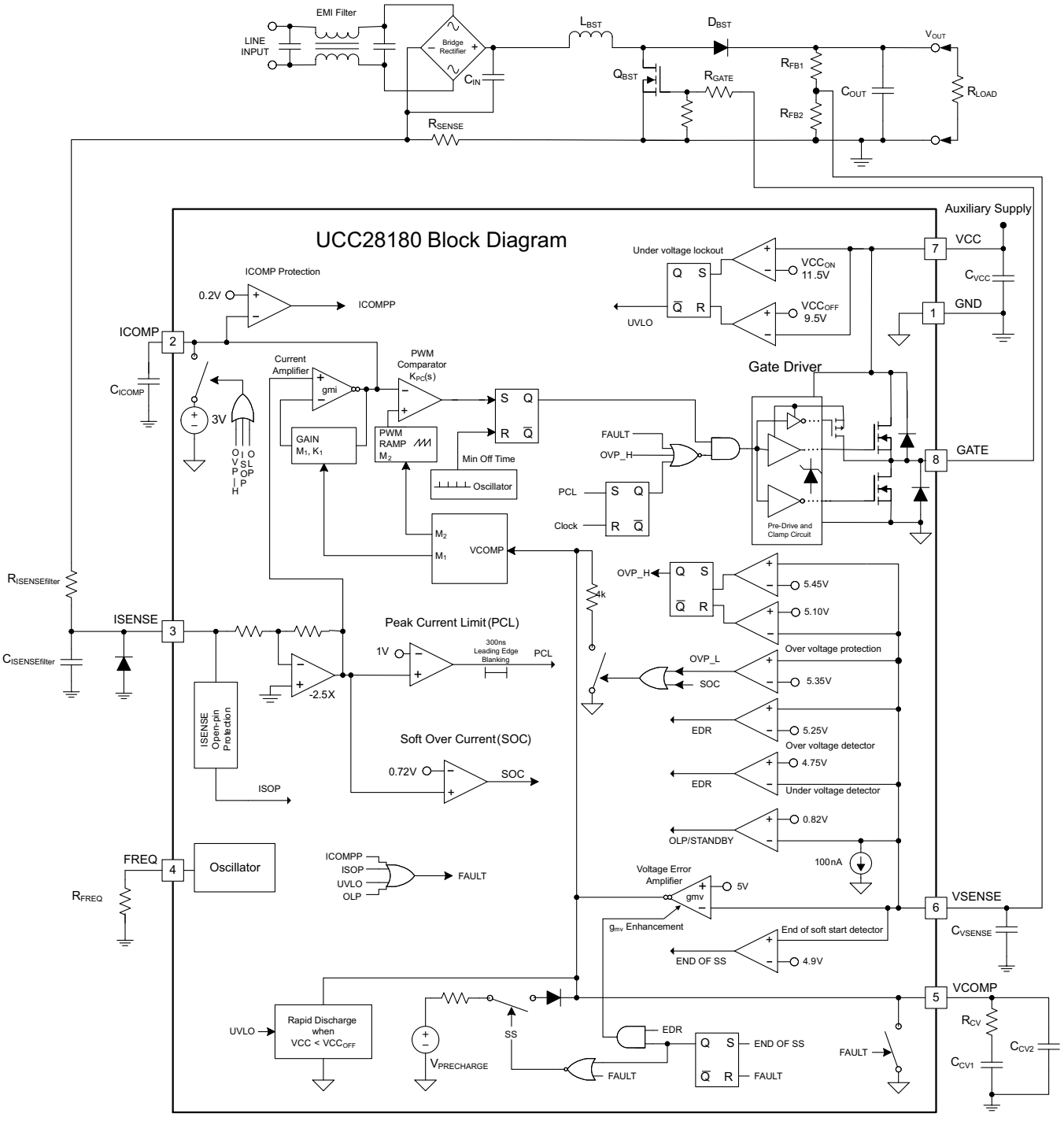
The UCC28180 is a boost controller for power factor correction operating at a fixed frequency in continuous conduction mode. The UCC28180 requires few external components to operate as an active PFC pre-regulator.

UCC28180 employs two control loops. An internal error amplifier and 5-V reference provide a slow outer loop to control output voltage. External compensation of this outer loop is applied by means of the VCOMP pin. The inner current loop shapes the average input current to match the sinusoidal input voltage. The inner current loop avoids the need to sense input voltage by exploiting the relationship between input voltage and boost duty-cycle. External compensation of the inner current loop is applied by means of the ICOMP pin.

The operating switching frequency can be programmed from 18 kHz to 250 kHz simply by connecting the FREQ pin to ground through a resistor.

UCC28180 includes a number of protection functions designed to ensure it is reliable, and will provide safe operation under all conditions, including abnormal or fault conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Soft Start

Soft-Start controls the rate of rise of VCOMP in order to obtain a linear control of the increasing duty cycle as a function of time. VCOMP, the output of the voltage loop transconductance amplifier, is pulled low during UVLO, ICOMPP, ISOP and OLP (Open-Loop Protection)/STANDBY. Once the fault condition is released, an initial pre-charge source rapidly charges VCOMP to 1.5 V. After that point, a constant 40 µA of current is sourced into the compensation components causing the voltage on this pin to ramp linearly until the output voltage reaches 85% of its final value. At this point, the sourcing current decreases until the output voltage reaches its final rated voltage. The soft-start time is controlled by the voltage error amplifier compensation capacitor values selected, and is user programmable based on desired loop crossover frequency. Once the output voltage exceeds 98% of rated voltage, soft start is over, the initial pre-charge source is disconnected, and EDR is no longer inhibited.

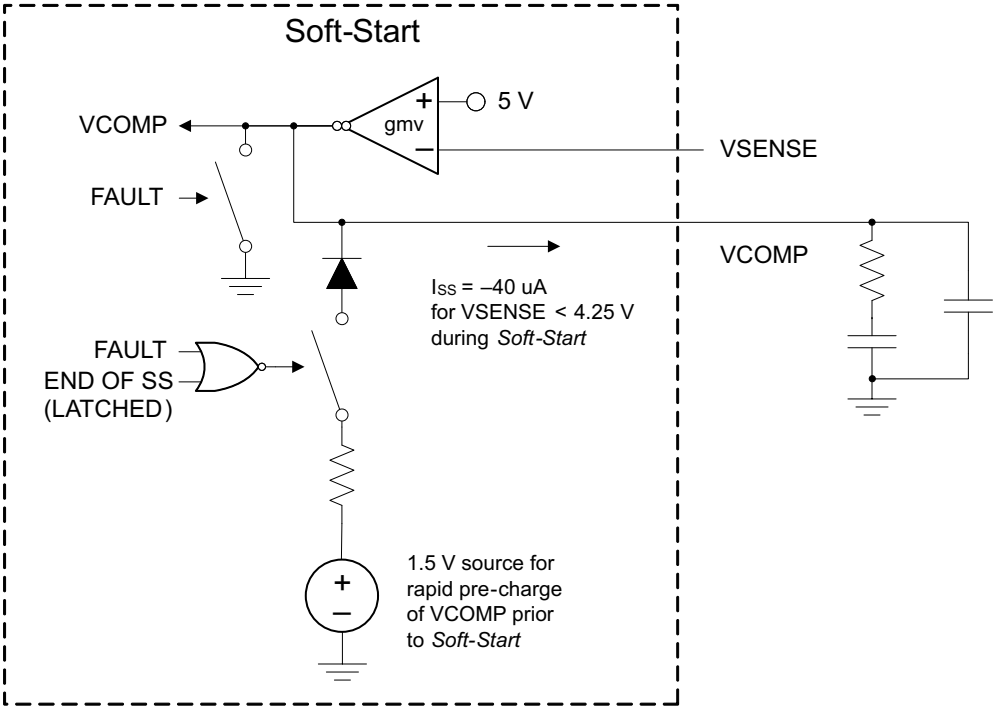


图 23. Soft Start

8.3.2 System Protection

System-level protection features help keep the system within safe operating limits.

8.3.3 VCC Undervoltage LockOut (UVLO)

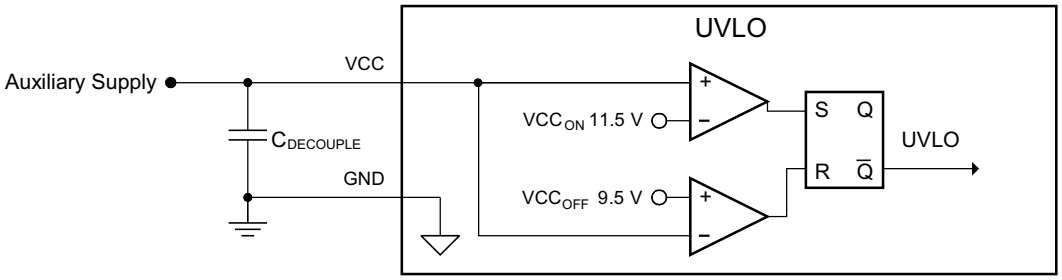


图 24. UVLO

Feature Description (接下页)

During startup, Under-Voltage LockOut (UVLO) keeps the device in the off state until VCC rises above the 11.5-V enable threshold, VCC_{ON}. With a typical 1.7 V of hysteresis on UVLO to increase noise immunity, the device turns off when VCC drops to the 9.5-V disable threshold, VCC_{OFF}.

If, during a brief AC-line dropout, the VCC voltage falls below the level necessary to bias the internal FAULT circuitry, the UVLO condition enables a special rapid discharge circuit which continues to discharge the VCOMP capacitors through a low impedance despite a complete lack of VCC. This helps to avoid an excessive current surge should the AC-line return while there is still substantial voltage stored on the VCOMP capacitors. Typically, these capacitors can be discharged to less than 1 V within 150 ms of loss of VCC.

8.3.4 Output Overvoltage Protection (OVP)

There are two levels of OVP: When VSENSE exceeds 107% (V_{OVP_L}) of the reference voltage, a 4-kΩ resistor connects VCOMP to ground to rapidly discharge VCOMP. If VSENSE exceeds 109% (V_{OVP_H}) of the reference voltage, GATE output is disabled until VSENSE drops below 102% of the reference voltage.

8.3.5 Open Loop Protection/Standby (OLP/Standby)

If the output voltage feedback components were to fail and disconnect (open loop) the signal from the VSENSE input, then it is likely that the voltage error amp would increase the GATE output to maximum duty cycle. To prevent this, an internal pull-down forces VSENSE low. If the output voltage falls below 16.5% of its rated voltage, causing VSENSE to fall below 0.82 V, the device is put in standby, a state where the PWM switching is halted and the device is still on but draws standby current below 2.95 mA. This shutdown feature also gives the designer the option of pulling VSENSE low with an external switch (standby function).

8.3.6 ISENSE Open-Pin Protection (ISOP)

If the current feedback components were to fail and disconnect (open loop) the signal to the ISENSE input, then it is likely that the PWM stage would increase the GATE output to maximum duty cycle. To prevent this, an internal pull-up source drives ISENSE above 0.085 V so that a detector forces a state where the PWM switching is halted and the device is still on but draws standby current below 2.95 mA. This shutdown feature avoids continual operation in OVP and severely distorted input current.

8.3.7 ICOMP Open-Pin Protection (ICOMPP)

If the ICOMP pin shorts to ground, then the GATE output increases to maximum duty cycle. To prevent this, once ICOMP pin voltage falls below 0.2 V, the PWM switching is halted and the device is still on but draws standby current below 2.95 mA .

8.3.8 FAULT Protection

VCC UVLO, OLP/Standby, ISOP and ICOMPP funtions constitute the fault protection feature in the UCC28180. Under fault protection, VCOMP pin is pulled low and the device is in standby.

8.3.9 Output Overvoltage Detection (OVD), Undervoltage Detection (UVD) and Enhanced Dynamic Response (EDR)

During normal operation, small perturbations on the PFC output voltage rarely exceed ±5% deviation and the normal voltage control loop gain drives the output back into regulation. For large changes in line or load, if the output voltage perturbation exceeds ±5%, an output over-voltage (OVD) or under-voltage (UVD) is detected and Enhanced Dynamic Response (EDR) acts to speed up the slow response of the low-bandwidth voltage loop. During EDR, the transconductance of the voltage error amplifier is increased approximately five times to speed charging or discharging the voltage-loop compensation capacitors to the level required for regulation. EDR is disabled when 5.25 V > VSENSE > 4.75 V. The EDR feature is not activated until soft start is completed. The UVD is disabled during soft over protection (SOC) condition (since UVD and SOC conflict with each other).

Feature Description (接下页)

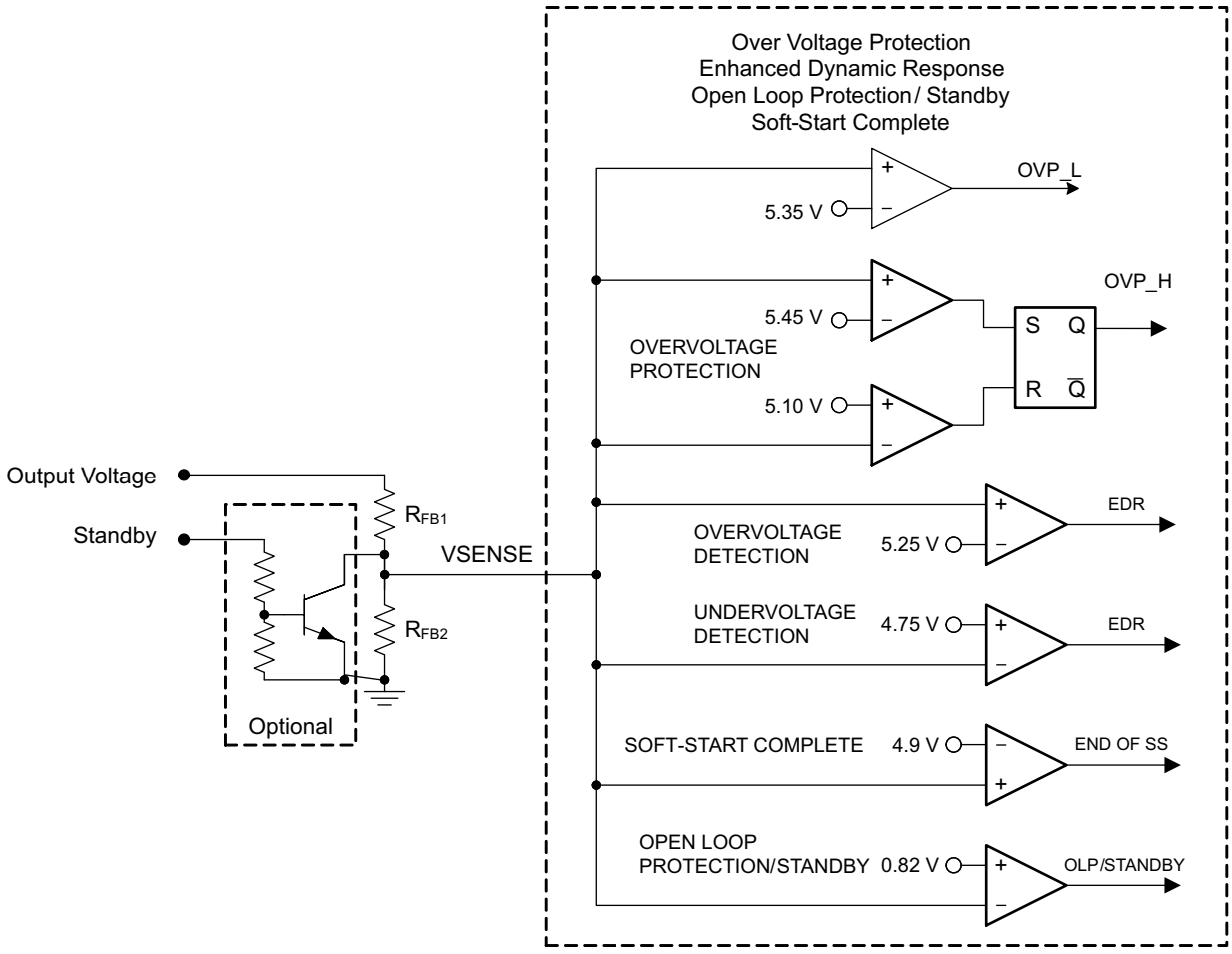


图 25. OVP_H, OVP_L, EDR, OLP, Soft Start Complete

8.3.10 Overcurrent Protection

Inductor current is sensed by R_{ISENSE}, a low value resistor in the return path of input rectifier. The other side of the resistor is tied to the system ground. The voltage is sensed on the rectifier side of the sense resistor and is always negative. The voltage at ISENSE is buffered by a fixed gain of -2.5 to provide a positive internal signal to the current functions. There are two overcurrent protection features; Soft Overcurrent (SOC) protects against an overload on the output and Peak Current Limit (PCL) protects against inductor saturation.

Feature Description (接下页)

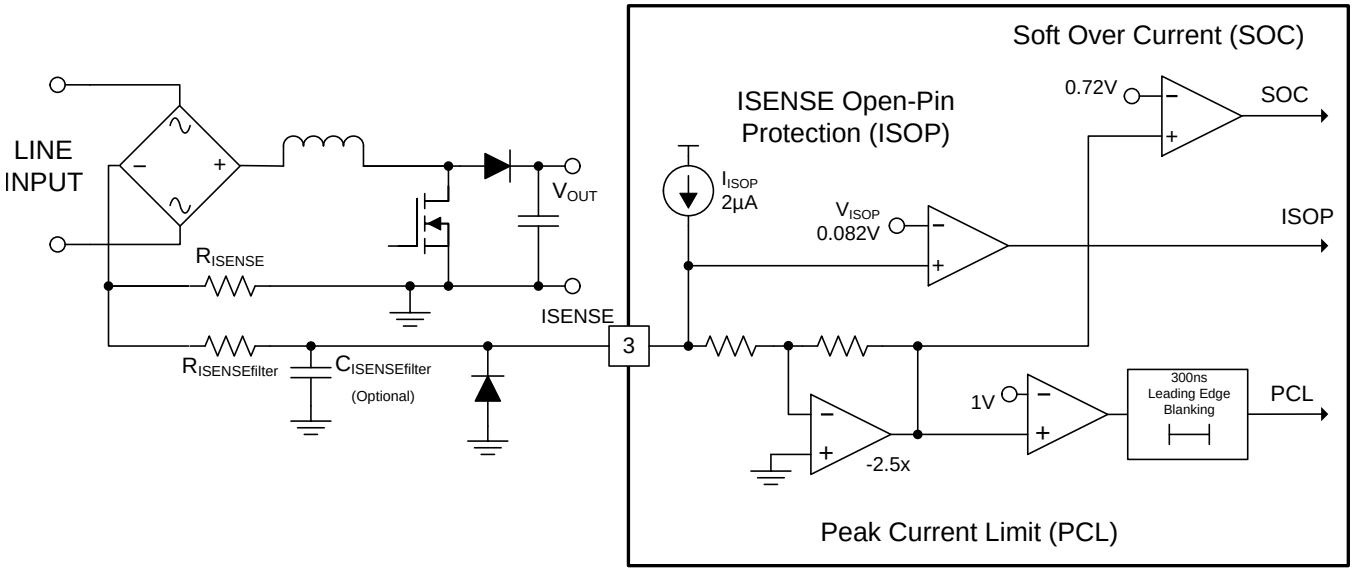


图 26. Soft Overcurrent/Peak-Current Limit

8.3.11 Soft Overcurrent (SOC)

Soft Overcurrent (SOC) limits the input current. SOC is activated when the current sense voltage on ISENSE reaches –0.285 V. This is a soft control as it does not directly switch off the gate driver. Instead a 4-kΩ resistor connects VCOMP to ground to discharge VCOMP and the control loop is adjusted to reduce the PWM duty cycle. The under-voltage detection (UVD) is disabled during SOC.

8.3.12 Peak Current Limit (PCL)

Peak Current Limit (PCL) operates on a cycle-by-cycle basis. When the current sense voltage on ISENSE reaches –0.4 V, PCL is activated, immediately terminating the active switch cycle. PCL is leading-edge blanked to improve noise immunity against false triggering.

8.3.13 Current Sense Resistor, R_{ISENSE}

The current sense resistor, R_{ISENSE}, is sized using the minimum threshold value of Soft Over Current (SOC), $V_{SOC(min)}$. To avoid triggering this threshold during normal operation, resulting in a decreased duty-cycle, the resistor is sized for an overload current of 10% more than the peak inductor current,

$$R_{ISENSE} \leq \frac{V_{SOC(min)}}{1.1\, I_{L\_PEAK(max)}} \quad (1)$$

Since R_{ISENSE} "sees" the average input current, worst-case power dissipation occurs at input low-line when input current is at its maximum. Power dissipated by the sense resistor is given by:

$$P_{RISENSE} = \left(I_{IN\_RMS(max)}\right)^2 R_{ISENSE} \quad (2)$$

Peak current limit (PCL) protection turns off the output driver when the voltage across the sense resistor reaches the PCL threshold, V_{PCL}. The absolute maximum peak current, $_{IPCL}$, is given by:

$$I_{PCL} = \frac{V_{PCL} / 2.5}{R_{ISENSE}} \quad (3)$$

Feature Description (接下页)

8.3.14 ISENSE Pin

The voltage at the ISENSE pin should be limited between 0 V and –1.1 V. Inrush currents at start-up have the potential to drive the ISENSE pin significantly more negative so a diode clamp should be used between ISENSE and GND to prevent the ISENSE pin going more negative than 1.1 V, (see 图 26). The diode Vf should be greater than the maximum PCL threshold (–0.438 V) and less than –1.1 V across temperature and component variations.

8.3.15 Gate Driver

The GATE output is designed with a current-optimized structure to directly drive large values of total MOSFET/IGBT gate capacitance at high turn-on and turn-off speeds. An internal clamp limits voltage on the MOSFET gate to 15.2 V (typical). When VCC voltage is below the UVLO level, the GATE output is held in the off state. An external gate drive resistor, R_{GATE}, can be used to limit the rise and fall times and dampen ringing caused by parasitic inductances and capacitances of the gate drive circuit and to reduce EMI. The final value of the resistor depends upon the parasitic elements associated with the layout and other considerations. A 10-kΩ resistor close to the gate of the MOSFET/IGBT, between the gate and ground, discharges stray gate capacitance and helps protect against inadvertent dv/dt-triggered turn-on.

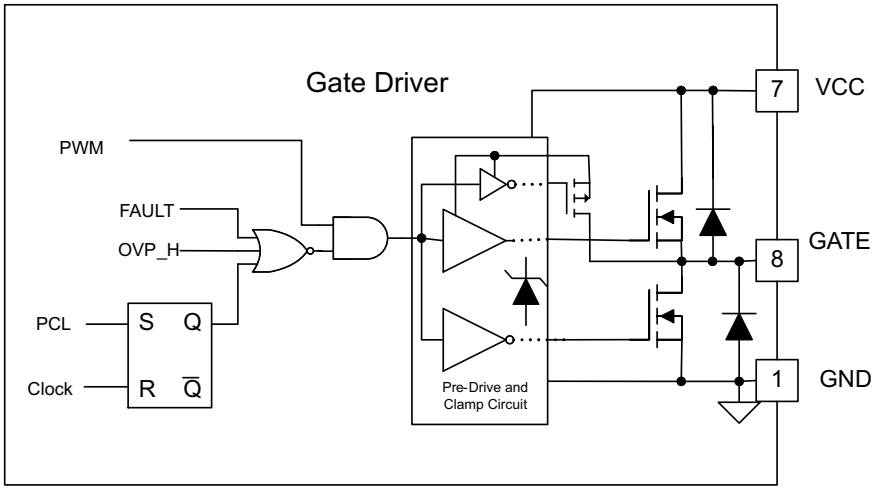


图 27. Gate Driver

8.3.16 Current Loop

The overall system current loop consists of the current averaging amplifier stage, the pulse width modulator (PWM) stage, the external boost inductor stage and the external current sensing resistor.

8.3.17 ISENSE and ICOMP Functions

The negative polarity signal from the current sense resistor is buffered and inverted at the ISENSE input. The internal positive signal is then averaged by the current amplifier (g_{mi}), whose output is the ICOMP pin. The voltage on ICOMP is proportional to the average inductor current. An external capacitor to GND is applied to the ICOMP pin for current loop compensation and current ripple filtering. The gain of the averaging amplifier is determined by the internal VCOMP voltage. This gain is non-linear to accommodate the world-wide AC-line voltage range.

ICOMP is connected to 3-V internally whenever OVP_H, ISOP, or OLP is triggered.

8.3.18 Pulse Width Modulator

The PWM stage compares the ICOMP signal with a periodic ramp to generate a leading-edge-modulated output signal which is high whenever the ramp voltage exceeds the ICOMP voltage. The slope of the ramp is defined by a non-linear function of the internal VCOMP voltage.

Feature Description (接下页)

The PWM output signal always starts low at the beginning of the cycle, triggered by the internal clock. The output stays low for a minimum off-time, t_{OFF_min}, after which the ramp rises linearly to intersect the ICOMP voltage. The ramp-ICOMP intersection determines t_{OFF}, and hence D_{OFF}. Since $D_{OFF} = V_{IN}/V_{OUT}$ by the boost-topology equation, and since V_{IN} is sinusoidal in wave-shape, and since ICOMP is proportional to the inductor current, it follows that the control loop forces the inductor current to follow the input voltage wave-shape to maintain boost regulation. Therefore, the average input current is also sinusoidal in wave-shape.

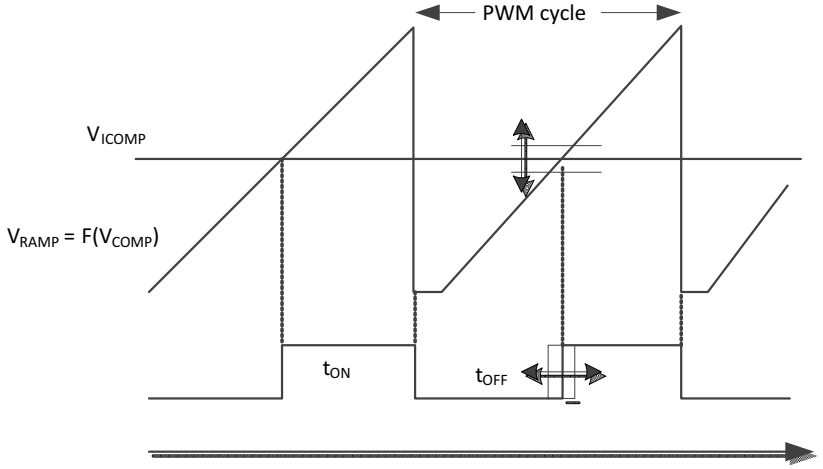


图 28. PWM Generation

8.3.19 Control Logic

The output of the PWM comparator stage is conveyed to the GATE drive stage, subject to control by various protection functions incorporated into the device. The GATE output duty-cycle may be as high as 98%, but always has a minimum off-time t_{OFF_min}. Normal duty-cycle operation can be interrupted directly by OVP_H and PCL. UVLO, ISOP, ICOMMP and OLP/Standby also terminate the GATE output pulse, and further inhibit output until the SS operation can begin.

8.3.20 Voltage Loop

The outer control loop of the PFC controller is the voltage loop. This loop consists of the PFC output sensing stage, the voltage error amplifier stage, and the non-linear gain generation.

8.3.21 Output Sensing

A resistor-divider network from the PFC output voltage to GND forms the sensing block for the voltage control loop. The resistor ratio is determined by the desired output voltage and the internal 5-V regulation reference voltage.

The very low bias current at the VSENSE input allows the choice of the highest practicable resistor values for lowest power dissipation and standby current. A small capacitor from VSENSE to GND serves to filter the signal in a high-noise environment. This filter time constant should generally be less than 100 µs.

8.3.22 Voltage Error Amplifier

The transconductance error amplifier (g_{mv}) generates an output current proportional to the difference between the voltage feedback signal at VSENSE and the internal 5-V reference. This output current charges or discharges the compensation network capacitors on the VCOMP pin to establish the proper VCOMP voltage for the system operating conditions. Proper selection of the compensation network components leads to a stable PFC pre-regulator over the entire AC-line range and 0% to 100% load range. The total capacitance also determines the rate-of-rise of the VCOMP voltage at *Soft Start*, as discussed earlier.

Feature Description (接下页)

The amplifier output VCOMP is pulled to GND during any fault or standby condition to discharge the compensation capacitors to an initial zero state. Usually, the large capacitor has a series resistor which delays complete discharge for their respective time constant (which may be several hundred milliseconds). If VCC bias voltage is quickly removed after UVLO, the normal discharge transistor on VCOMP loses drive and the large capacitor could be left with substantial voltage on it, negating the benefit of a subsequent *Soft Start.* The UCC28180 incorporates a parallel discharge path which operates without VCC bias, to further discharge the compensation network after VCC is removed.

If the output voltage perturbations exceed ±5%, and output over-voltage (OVD) or under-voltage (UVD) is detected, the OVD or UVD function invokes EDR which immediately increases the voltage error amplifier transconductance to about 280 µS. This higher gain facilitates faster charging or discharging the compensation capacitors to the new operating level. When output voltage perturbations greater than 107%V_{REF} appear at the VSENSE input, a 4-kΩ resistor connects VCOMP to ground to quickly reduce VCOMP voltage. When output voltage perturbations are greater than 109%V_{REF}, the GATE output is shut off until VSENSE drops below 102% of regulation.

8.3.23 Non-Linear Gain Generation

The voltage at VCOMP is used to set the current amplifier gain and the PWM ramp slope. This voltage is subject to modification by the SOC function, as discussed earlier.

Together the current gain and the PWM slope adjust to the different system operating conditions (set by the AC-line voltage and output load level) as VCOMP changes, to provide a low-distortion, high-power-factor, input-current wave shape following that of the input voltage.

8.4 Device Functional Modes

This device has no functional modes.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The UCC28180 is a switch-mode controller used in boost converters for power factor correction operating at a fixed frequency in continuous conduction mode. The UCC28180 requires few external components to operate as an active PFC pre-regulator. The operating switching frequency can be programmed from 18 kHz to 250 kHz simply by connecting the FREQ pin to ground through a resistor.

The internal 5-V reference voltage provides for accurate output voltage regulation over the typical world-wide 85-VAC to 265-VAC mains input range from zero to full output load. The usable system load ranges from 100 W to few kW.

Regulation is accomplished in two loops. The inner current loop shapes the average input current to match the sinusoidal input voltage under continuous inductor current conditions. Under light-load conditions, depending on the boost inductor value, the inductor current may go discontinuous but still meet Class-A/D requirements of IEC 61000-3-2 despite the higher harmonics. The outer voltage loop regulates the PFC output voltage by generating a voltage on VCOMP (dependent upon the line and load conditions) which determines the internal gain parameters for maintaining a low-distortion, steady-state, input-current wave shape.

9.2 Typical Application

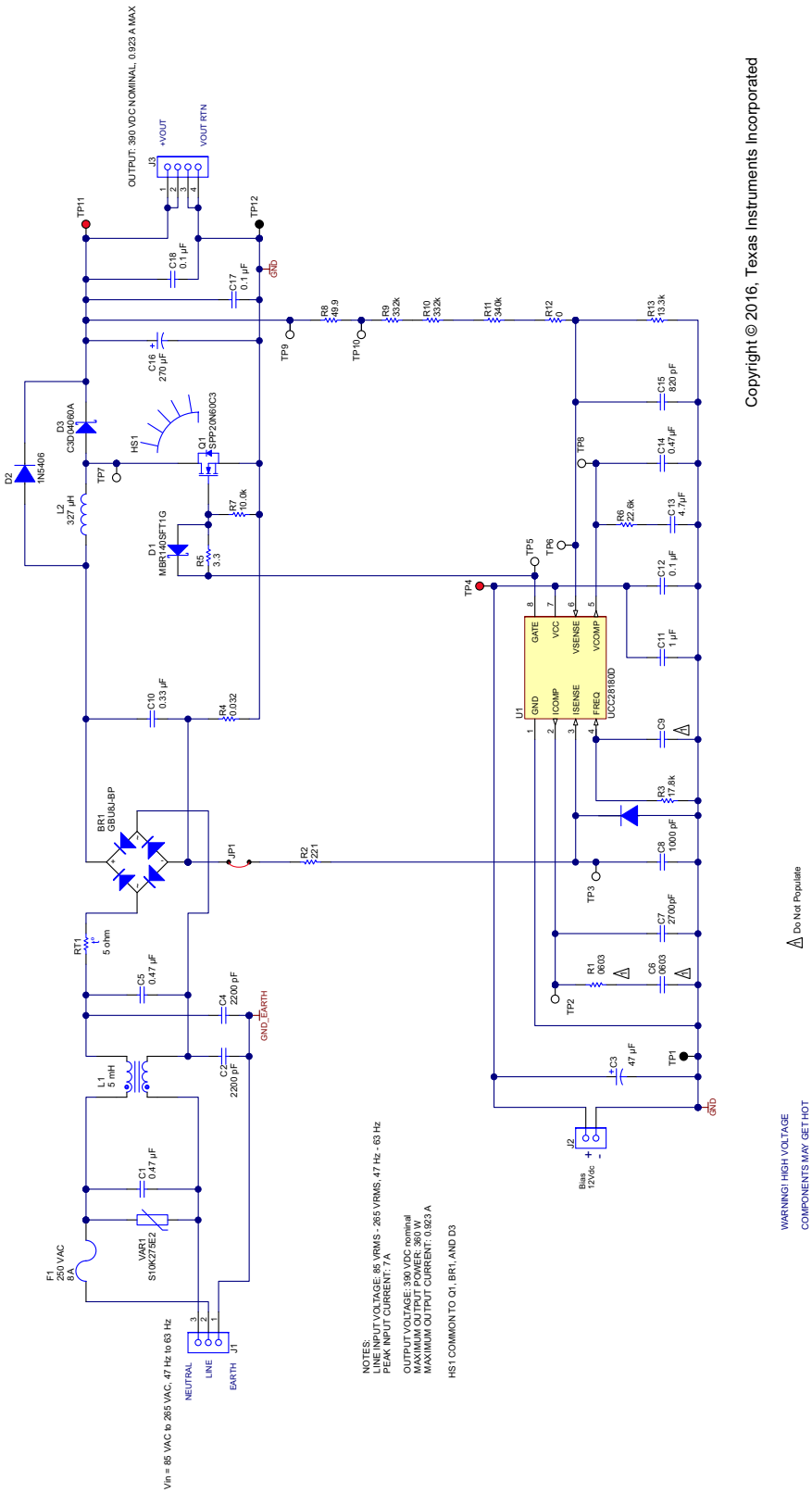


图 29. Design Example Schematic

Typical Application (接下页)

9.2.1 Design Requirements

This example illustrates the design process and component selection for a continuous mode power factor correction boost converter utilizing the UCC28180. The pertinent design equations are shown for a universal input, 360-W PFC converter with an output voltage of 390 V.

表 1. Design Goal Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		85		265	V_{AC}
f_{LINE}	Input frequency		47		63	Hz
$I_{IN(peak)}$	Peak input current	$V_{IN} = V_{IN(min)}$, $I_{OUT} = I_{OUT(max)}$		7		A
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$, $I_{OUT} \le I_{OUT(max)}$	379	390	402	VDC
	Line Regulation	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$, $I_{OUT} = I_{OUT(max)}$			5%	
	Load Regulation	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, $I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$			5%	
		V_{IN} = 230 VAC, f_{LINE} = 60 Hz, $I_{OUT(min)} \le I_{OUT} \le I_{OUT(max)}$			5%	
I_{OUT}	Output Load Current	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$	0		0.923	A
P_{OUT}	Output Power	$V_{IN(min)} \le V_{IN} \le V_{IN(max)}$ $f_{LINE(min)} \le f_{LINE} \le f_{LINE(max)}$	0		360	W
$V_{RIPPLE(SW)}$	High frequency Output voltage ripple	V_{IN} = 115 VAC, f_{LINE} = 60 Hz $I_{OUT} = I_{OUT(max)}$		2.5	3.9	V_{P-P}
		V_{IN} = 230 VAC, f_{LINE} = 50 Hz $I_{OUT} = I_{OUT(max)}$		2.5	3.9	
$V_{RIPPLE(f\_LINE)}$	Line frequency Output voltage ripple	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, $I_{OUT} = I_{OUT(max)}$		11.6	19.5	V_{P-P}
		V_{IN} = 230 VAC, f_{LINE} = 50 Hz, $I_{OUT} = I_{OUT(max)}$		13.3	19.5	
$V_{OUT(OVP)}$	Output overvoltage protection			425		V
$V_{OUT(UVP)}$	Output undervoltage protection			370		

Typical Application (接下页)

表 1. Design Goal Parameters (接下页)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CONTROL LOOP CHARACTERISTICS						
f_{SW}	Switching frequency	T_J = 25°C	114	120	126	kHz
$f_{(CO)}$	Voltage Loop Bandwidth	V_{IN} = 162 VDC, I_{OUT} = 0.466 A		8		Hz
	Voltage Loop Phase Margin	V_{IN} = 162 VDC, I_{OUT} = 0.466 A		68		°
PF	Power Factor	V_{IN} = 115 VAC, I_{OUT} = $I_{OUT(max)}$		0.99		
THD	Total harmonic distortion	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = $I_{OUT(max)}$		4.3%	10%	
		VIN = 230 VAC, f_{LINE} = 50 Hz I_{OUT} = $I_{OUT(max)}$		4%	10%	
η	Full load efficiency	V_{IN} = 115 VAC, f_{LINE} = 60 Hz, I_{OUT} = $I_{OUT(max)}$		94%		
	Ambient temperature			25		°C

9.2.2 Detailed Design Procedure

9.2.2.1 Current Calculations

The input fuse, bridge rectifier, and input capacitor are selected based upon the input current calculations. First, determine the maximum average output current, $I_{OUT(max)}$:

$$I_{OUT(max)} = \frac{P_{OUT(max)}}{V_{OUT}} \quad (4)$$

$$I_{OUT(max)} = \frac{360\,W}{390\,V} \cong 0.923\,A \quad (5)$$

The maximum input RMS line current, $I_{IN\_RMS(max)}$, is calculated using the parameters from 表 1 and the efficiency and power factor initial assumptions:

$$I_{IN\_RMS(max)} = \frac{P_{OUT(max)}}{\eta V_{IN(min)} PF} \quad (6)$$

$$I_{IN\_RMS(max)} = \frac{360\,W}{0.94 \times 85\,V \times 0.99} = 4.551A \quad (7)$$

Based upon the calculated RMS value, the maximum input current, $I_{IN\ (max)}$, and the maximum average input current, $I_{IN\_AVG(max)}$, assuming the waveform is sinusoidal, can be determined.

$$I_{IN(max)} = \sqrt{2} I_{IN\_RMS(max)} \quad (8)$$

$$I_{IN(max)} = \sqrt{2} \times 4.551A = 6.436\,A \quad (9)$$

$$I_{IN\_AVG(max)} = \frac{2 I_{IN(max)}}{\pi} \quad (10)$$

$$I_{IN\_AVG(max)} = \frac{2 \times 6.436\,A}{\pi} = 4.097\,A \quad (11)$$

9.2.2.2 Switching Frequency

The UCC28180 switching frequency is user programmable with a single resistor on the FREQ pin to ground. For this design, the switching frequency, f_{SW}, was chosen to be 120 kHz. 图 30 (same as 图 1) could be used to select the suitable resistor to program the switching frequency or the value can be calculated using constant scaling values of f_{TYP} and R_{TYP}. In all cases, f_{TYP} is a constant that is equal to 65 kHz, R_{INT} is a constant that is equal to 1 MΩ, and R_{TYP} is a constant that is equal to 32.7 kΩ. Simply applying the calculation below yields the appropriate resistor that should be placed between FREQ and GND:

$$R_{FREQ} = \frac{f_{TYP} \times R_{TYP} \times R_{INT}}{(f_{SW} \times R_{INT}) + (R_{TYP} \times f_{SW}) - (R_{TYP} \times f_{TYP})} \quad (12)$$

$$R_{FREQ} = \frac{65\,kHz \times 32.7\,k\Omega \times 1M\Omega}{(120\,kHz \times 1M\Omega) + (32.7\,k\Omega \times 120\,kHz) - (32.7\,k\Omega \times 65\,kHz)} = 17.451k\Omega \quad (13)$$

A typical value of 17.8 kΩ for the FREQ resistor results in a switching frequency of 118 kHz.

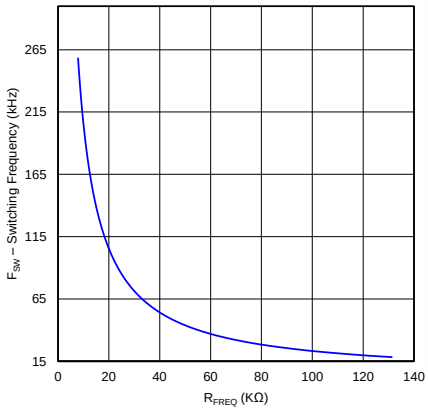


图 30. Frequency vs. R_{FREQ}

9.2.2.3 Bridge Rectifier

The input bridge rectifier must have an average current capability that exceeds the input average current. Assuming a forward voltage drop, V_{F_BRIDGE}, of 1 V across the rectifier diodes, BR1, the power loss in the input bridge, P_{BRIDGE}, can be calculated:

$$P_{BRIDGE} = 2 V_{F\_BRIDGE} I_{IN\_AVG(max)} \quad (14)$$

$$P_{BRIDGE} = 2 \times 1V \times 4.097\,A = 8.195\,W \quad (15)$$

Heat sinking will be required to maintain operation within the bridge rectifier's safe operating area.

9.2.2.4 Inductor Ripple Current

The UCC28180 is a Continuous Conduction Mode (CCM) controller but if the chosen inductor allows relatively high-ripple current, the converter will be forced to operate in Discontinuous Mode (DCM) at light loads and at the higher input voltage range. High-inductor ripple current has an impact on the CCM/DCM boundary and results in higher light-load THD, and also affects the choices for the input capacitor, R_{SENSE} and C_{ICOMP} values. Allowing an inductor ripple current, ΔI_{RIPPLE}, of 20% or less will result in CCM operation over the majority of the operating range but requires a boost inductor that has a higher inductance value and the inductor itself will be physically large. As with all converter designs, decisions must be made at the onset in order to optimize performance with size and cost. In this design example, the inductor is sized in such a way as to allow a greater amount of ripple current in order to minimize space with the understanding that the converter operates in DCM at the higher input voltages and at light loads but optimized for a nominal input voltage of 115 V_{AC} at full load. Although specifically defined as a CCM controller, the UCC28180 is shown in this application to meet the overall performance goals while transitioning into DCM at high-line voltage, at a higher load level.

9.2.2.5 Input Capacitor

The input capacitor must be selected based upon the input ripple current and an acceptable high frequency input voltage ripple. Allowing an inductor ripple current, ΔI_{RIPPLE}, of 40% and a high frequency voltage ripple factor, ΔV_{RIPPLE_IN}, of 7%, the maximum input capacitor value, C_{IN}, is calculated by first determining the input ripple current, I_{RIPPLE}, and the input voltage ripple, V_{IN_RIPPLE}:

$$I_{RIPPLE} = \Delta I_{RIPPLE} I_{IN(max)} \tag{16}$$

$$\Delta I_{RIPPLE} = 0.4 \tag{17}$$

$$I_{RIPPLE} = 0.4 \times 6.436\,A = 2.575\,A \tag{18}$$

$$V_{IN\_RIPPLE} = \Delta V_{RIPPLE\_IN} V_{IN\_RECTIFIED(min)} \tag{19}$$

$$\Delta V_{RIPPLE\_IN} = 0.07 \tag{20}$$

$$V_{IN\_RECTIFIED} = \sqrt{2} V_{IN} \tag{21}$$

$$V_{IN\_RECTIFIED} = \sqrt{2} \times 85\,V = 120\,V \tag{22}$$

$$V_{IN\_RIPPLE} = 0.07 \times 120\,V = 8.415\,V \tag{23}$$

The recommended value for the input x-capacitor can now be calculated:

$$C_{IN} = \frac{I_{RIPPLE}}{8 f_{SW} V_{IN\_RIPPLE}} \tag{24}$$

$$C_{IN} = \frac{2.575\,A}{8 \times 118\,kHz \times 8.415\,V} = 0.324\,\mu F \tag{25}$$

A standard value 0.33-µF Y2/X2 film capacitor is used.

9.2.2.6 Boost Inductor

Based upon the allowable inductor ripple current discussed above, the boost inductor, L_{BST}, is selected after determining the maximum inductor peak current, I_{L_PEAK}:

$$I_{L\_PEAK(max)} = I_{IN(max)} + \frac{I_{RIPPLE}}{2} \tag{26}$$

$$I_{L\_PEAK(max)} = 6.436\,A + \frac{2.575\,A}{2} = 7.724\,A \tag{27}$$

The minimum value of the boost inductor is calculated based upon the acceptable ripple current, I_{RIPPLE}, at a worst case duty cycle of 0.5:

$$L_{BST(min)} \geq \frac{V_{OUT} D(1-D)}{f_{SW} I_{RIPPLE}} \tag{28}$$

$$L_{BST(min)} \geq \frac{390\,V \times 0.5(1-0.5)}{118\,kHz \times 2.575\,A} \geq 321\,\mu H \tag{29}$$

The recommended minimum value for the boost inductor assuming a 40% ripple current is 321 µH; the actual value of the boost inductor that will be used is 327 µH. With this actual value used, the actual resultant inductor current ripple will be:

$$L_{BST} = 327\,\mu H \tag{30}$$

$$I_{RIPPLE(actual)} = \frac{V_{OUT} D(1-D)}{f_{SW} L_{BST}} \tag{31}$$

$$I_{RIPPLE(actual)} = \frac{390\,V \times 0.5(1-0.5)}{118\,kHz \times 327\,\mu H} = 2.527\,A \tag{32}$$

$$I_{L\_PEAK(max)} = 6.436\,A + \frac{2.527\,A}{2} = 7.7\,A \tag{33}$$

The duty cycle is a function of the rectified input voltage and will be continuously changing over the half line cycle. The duty cycle, $DUTY_{(max)}$, can be calculated at the peak of the minimum input voltage:

$$DUTY_{(max)} = \frac{V_{OUT} - V_{IN\_RECTIFIED(min)}}{V_{OUT}} \quad (34)$$

$$V_{IN\_RECTIFIED(min)} = \sqrt{2} \times 85\,V = 120\,V \quad (35)$$

$$DUTY_{(max)} = \frac{390\,V - 120\,V}{390\,V} = 0.692 \quad (36)$$

9.2.2.7 Boost Diode

The diode losses are estimated based upon the forward voltage drop, V_F, at 125°C and the reverse recovery charge, Q_{RR}, of the diode. Using a silicon carbide Schottky diode, although more expensive, will essentially eliminate the reverse recovery losses and result in less power dissipation:

$$P_{DIODE} = V_{F\_125C} I_{OUT(max)} + 0.5 f_{SW} V_{OUT} Q_{RR} \quad (37)$$

$$V_{F\_125°C} = 1V \quad (38)$$

$$Q_{RR} = 0nC \quad (39)$$

$$P_{DIODE} = (1V \times 0.923\,A) + (0.5 \times 119kHz \times 390\,V \times 0nC) = 0.923\,W \quad (40)$$

This output diode should have a blocking voltage that exceeds the output over voltage of the converter and be attached to an appropriately sized heat sink.

9.2.2.8 Switching Element

The MOSFET/IGBT switch will be driven by a GATE output that is clamped at 15.2 V for VCC bias voltages greater than 15.2 V. An external gate drive resistor is recommended to limit the rise time and to dampen any ringing caused by the parasitic inductances and capacitances of the gate drive circuit; this will also help in meeting any EMI requirements of the converter. The design example uses a 3.3-Ω resistor; the final value of any design is dependent upon the parasitic elements associated with the layout of the design. To facilitate a fast turn off, a standard 40-V, 1-A Schottky diode is placed anti-parallel with the gate drive resistor. A 10-kΩ resistor is placed between the gate of the MOSFET/IGBT and ground to discharge the gate capacitance and protect from inadvertent dv/dt triggered turn-on.

The conduction losses of the switch MOSFET, in this design are estimated using the $R_{DS(on)}$ at 125°C, found in the device data sheet, and the calculated drain to source RMS current, I_{DS_RMS}:

$$P_{COND} = I_{DS\_RMS}^2 R_{DS(on)125°C} \quad (41)$$

$$R_{DS(on)125°C} = 0.35\,\Omega \quad (42)$$

$$I_{DS\_RMS} = \frac{P_{OUT(max)}}{V_{IN\_RECTIFIED(min)}} \sqrt{2 - \frac{16 V_{IN\_RECTIFIED(min)}}{3\pi V_{OUT}}} \quad (43)$$

$$I_{DS\_RMS} = \frac{360\,W}{120\,V} \sqrt{2 - \frac{16 \times 120\,V}{3\pi \times 390\,V}} = 3.639\,A \quad (44)$$

$$P_{COND} = 3.639\,A^2 \times 0.35\,\Omega = 4.636\,W \quad (45)$$

The switching losses are estimated using the rise time, tr, and fall time, t_f, of the MOSFET gate, and the output capacitance losses.

$$t_r = 5ns$$
$$t_f = 4.5ns$$
$$C_{OSS} = 780pF \quad (46)$$

$$P_{SW} = f_{SW}\left[0.5 V_{OUT} I_{IN(max)}(t_r + t_f) + 0.5 C_{OSS} V_{OUT}^2\right] \quad (47)$$

$$P_{SW} = 118kHz\left[0.5 \times 390\,V \times 6.436A(5ns + 4.5ns) + 0.5 \times 780pF \times 390\,V^2\right] = 8.407\,W \quad (48)$$

Total FET losses

$$P_{COND} + P_{SW} = 4.636\,W + 8.407\,W = 13.042\,W \quad (49)$$

The MOSFET requires an appropriately sized heat sink.

9.2.2.9 Sense Resistor

To accommodate the gain of the non-linear power limit, the sense resistor, R_{SENSE}, is sized such that it triggers the soft over current at 10% higher than the maximum peak inductor current using the minimum soft over current threshold of the ISENSE pin, V_{SOC}, of ISENSE equal to 0.265 V.

$$R_{SENSE} = \frac{V_{SOC(min)}}{I_{L\_PEAK(max)} \times 1.1} \quad (50)$$

$$R_{SENSE} = \frac{0.259\,V}{7.7\,A \times 1.1} = 0.032\,\Omega \quad (51)$$

The power dissipated across the sense resistor, P_{RSENSE}, must be calculated:

$$P_{RSENSE} = I^2_{IN\_RMS(max)} R_{SENSE} \quad (52)$$

$$P_{RSENSE} = 4.551\,A^2 \times 0.032\,\Omega = 0.663\,W \quad (53)$$

The peak current limit, PCL, protection feature is triggered when current through the sense resistor results in the voltage across R_{SENSE} to be equal to the V_{PCL} threshold. For a worst case analysis, the maximum V_{PCL} threshold is used:

$$I_{PCL} = \frac{V_{PCL(max)}}{R_{SENSE}} \quad (54)$$

$$I_{PCL} = \frac{0.438\,V}{0.032\,\Omega} = 13.688\,A \quad (55)$$

To protect the device from inrush current, a standard 220-Ω resistor, R_{ISENSE}, is placed in series with the ISENSE pin. A 1000-pF capacitor is placed close to the device to improve noise immunity on the ISENSE pin.

9.2.2.10 Output Capacitor

The output capacitor, C_{OUT}, is sized to meet holdup requirements of the converter. Assuming the downstream converters require the output of the PFC stage to never fall below 300 V, $V_{OUT\_HOLDUP(min)}$, during one line cycle, $t_{HOLDUP} = 1/f_{LINE(min)}$, the minimum calculated value for the capacitor is:

$$C_{OUT(min)} \geq \frac{2P_{OUT(max)} t_{HOLDUP}}{V^2_{OUT} - V^2_{OUT\_HOLDUP(min)}} \quad (56)$$

$$C_{OUT(min)} \geq \frac{2 \times 360\,W \times 21.28\,ms}{390\,V^2 - 300\,V^2} \geq 247\,\mu F \quad (57)$$

It is advisable to de-rate this capacitor value by 10%; the actual capacitor used is 270 µF.

Verifying that the maximum peak-to-peak output ripple voltage will be less than 5% of the output voltage ensures that the ripple voltage will not trigger the output over-voltage or output under-voltage protection features of the controller. If the output ripple voltage is greater than 5% of the regulated output voltage, a larger output capacitor is required. The maximum peak-to-peak ripple voltage, occurring at twice the line frequency, and the ripple current of the output capacitor is calculated:

$$V_{OUT\_RIPPLE(pp)} < 0.05\,V_{OUT} \quad (58)$$

$$V_{OUT\_RIPPLE(pp)} < 0.05 \times 390\,V = 19.5\,V_{PP} \quad (59)$$

$$V_{OUT\_RIPPLE(pp)} = \frac{I_{OUT}}{2\pi(2f_{LINE(min)})C_{OUT}} \quad (60)$$

$$V_{OUT\_RIPPLE(pp)} = \frac{0.923A}{2\pi(2 \times 47\,Hz) \times 270\,\mu F} = 5.789\,V \quad (61)$$

The required ripple current rating at twice the line frequency is equal to:

$$I_{COUT\_2fline} = \frac{I_{OUT(max)}}{\sqrt{2}} \quad (62)$$

$$I_{COUT\_2fline} = \frac{0.923\,A}{\sqrt{2}} = 0.653\,A \quad (63)$$

There is a high frequency ripple current through the output capacitor:

$$I_{COUT\_HF} = I_{OUT(max)} \sqrt{\frac{16\,V_{OUT}}{3\pi V_{IN\_RECTIFIED(min)}} - 1.5} \quad (64)$$

$$I_{COUT\_HF} = 0.923\,A \sqrt{\frac{16 \times 390\,V}{3\pi \times 120\,V} - 1.5} = 1.848\,A \quad (65)$$

The total ripple current in the output capacitor is the combination of both and the output capacitor must be selected accordingly:

$$I_{COUT\_RMS(total)} = \sqrt{I^2_{COUT\_2fline} + I^2_{COUT\_HF}} \quad (66)$$

$$I_{COUT\_RMS(total)} = \sqrt{0.653\,A^2 + 1.848\,A^2} = 1.96\,A \quad (67)$$

9.2.2.11 Output Voltage Set Point

For low power dissipation and minimal contribution to the voltage set point, it is recommended to use 1 MΩ for the top voltage feedback divider resistor, R_{FB1}. Multiple resistors in series are used due to the maximum allowable voltage across each. Using the internal 5-V reference, V_{REF}, the bottom divider resistor, R_{FB2}, is selected to meet the output voltage design goals.

$$R_{FB2} = \frac{V_{REF} R_{FB1}}{V_{OUT} - V_{REF}} \quad (68)$$

$$R_{FB2} = \frac{5\,V \times 1M\Omega}{390\,V - 5\,V} = 13.04\,k\Omega \quad (69)$$

A standard value 13-kΩ resistor for R_{FB2} results in a nominal output voltage set point of 391 V.

An output over voltage is detected when the output voltage exceeds its nominal set-point level by 5%, as measured when the voltage at VSENSE is 105% of the reference voltage, V_{REF}. At this threshold, the enhanced dynamic response (EDR) is triggered and the non-linear gain to the voltage error amplifier will increase the transconductance to VCOMP and quickly return the output to its normal regulated value. This EDR threshold occurs when the output voltage reaches the $V_{OUT(ovd)}$ level:

$$V_{OVD} = 1.05\,V_{REF} = 1.05 \times 5\,V = 5.25\,V \quad (70)$$

$$V_{OUT(ovd)} = V_{OVD}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) \quad (71)$$

$$V_{OUT(ovd)} = 5.25\,V \times \left(\frac{1M\Omega + 13\,k\Omega}{13\,k\Omega}\right) = 410.7\,V \quad (72)$$

In the event of an extreme output over voltage event, the GATE output will be disabled if the output voltage exceeds its nominal set-point value by 9%. The output voltage, $V_{OUT(ovp)}$, at which this protection feature is triggered is calculated as follows:

$$V_{OUT(ovp)} = 1.09 \times V_{REF}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) = 426.4\,V \quad (73)$$

An output under voltage is detected when the output voltage falls below 5% below its nominal set-point as measured when the voltage at VSENSE is 95% of the reference voltage, V_{REF}:

$$V_{UVD} = 0.95\,V_{REF} = 0.95 \times 5\,V = 4.75\,V \quad (74)$$

$$V_{OUT(uvp)} = V_{UVD}\left(\frac{R_{FB1} + R_{FB2}}{R_{FB2}}\right) \quad (75)$$

$$V_{OUT(uvp)} = 4.75\,V \times \left(\frac{1M\Omega + 13k\Omega}{13k\Omega}\right) = 371.6\,V \quad (76)$$

A small capacitor on VSENSE must be added to filter out noise. Limit the value of the filter capacitor such that the RC time constant is limited to approximately 10 µs so as not to significantly reduce the control response time to output voltage deviations.

$$C_{VSENSE} = \frac{10\mu s}{R_{FB2}} = 769\,pF \quad (77)$$

The closest standard value of 820 pF was used on VSENSE for a time constant of 10.66 µs.

9.2.2.12 Loop Compensation

The current loop is compensated first by determining the product of the internal loop variables, M_1M_2, using the internal controller constants K_1 and K_{FQ}. Compensation is optimized maximum load and nominal input voltage, 115 V_{AC} is used for the nominal line voltage for this design:

$$M_1M_2 = \frac{I_{OUT(max)} V_{OUT}^2 2.5 R_{SENSE} K_1}{\eta V_{IN\_RMS}^2 K_{FQ}} \quad (78)$$

$$K_{FQ} = \frac{1}{f_{SW}}$$

$$K_{FQ} = \frac{1}{118\,kHz} = 8.475\,\mu s$$

$$K_1 = 7 \quad (79)$$

$$M_1M_2 = \frac{0.923\,A \times 390\,V^2 \times 2.5 \times 0.032\,\Omega \times 7}{0.92 \times 115\,V^2 \times 8.475\,\mu s} = 0.751\frac{V}{\mu s} \quad (80)$$

The VCOMP operating point is found on the following chart, M_1M_2 vs. VCOMP. Once the M_1M_2 result is calculated above, find the resultant VCOMP voltage at that operating point to calculate the individual M_1 and M_2 components.

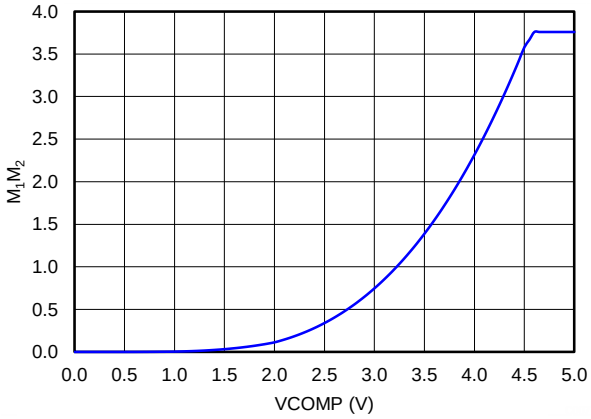


图 31. M1M2 vs. VCOMP

For the given M_1M_2 of 0.751 V/µs, the VCOMP approximately equal to 3 V, as shown in 图 31.

The individual loop factors, M_1 which is the current loop gain factor, and M_2 which is the voltage loop PWM ramp slope, are calculated using the following conditions:

The M_1 non-linear current loop gain factor follows the following identities:

$$M_1 = 0.068 \text{ if } V_{COMP} < 1 \text{ V} \quad (81)$$

$$M_1 = 0.156 \times VCOMP - 0.088 \text{ if } 1 \text{ V} < V_{COMP} < 2 \text{ V} \quad (82)$$

$$M_1 = 0.313 \times VCOMP - 0.401 \text{ if } 2 \text{ V} < V_{COMP} < 4.5 \text{ V} \quad (83)$$

$$M_1 = 1.007 \text{ if } 4.5 \text{ V} < V_{COMP} < 5 \text{ V} \quad (84)$$

In this example, according to the chart in 图 31, VCOMP is approximately equal to 3 V, so M1 is calculated to be approximately equal to 0.366:

$$M_1 = 0.313 \times 2.45 - 0.401 = 0.366 \quad (85)$$

The M_2 non-linear PWM ramp slope will obey the following relationships:

$$M_2 = 0 \frac{V}{\mu s} \text{ if } V_{COMP} \le 0.5 \text{ V} \quad (86)$$

$$M_2 = \frac{f_{SW}}{65 kHz} \times 0.1223 \times (VCOMP - 0.5)^2 \frac{V}{\mu s} \text{ if } 0.5 \text{ V} \le V_{COMP} \le 4.6 \text{ V} \quad (87)$$

$$M_2 = \frac{f_{SW}}{65 kHz} \times 2.056 \frac{V}{\mu s} \text{ if } 4.6 \text{ V} \le V_{COMP} \le 5 \text{ V} \quad (88)$$

In this example, with VCOMP approximately equal to 3 V, M_2 equals 1.388 V/µs:

$$M_2 = \frac{118 kHz}{65 kHz} \times 0.1223 \times (3 - 0.5)^2 \frac{V}{\mu s} = 1.388 \frac{V}{\mu s} \quad (89)$$

Verify that the product of the individual gain factors, M_1 and M_2, is approximately equal to the M_1M_2 factor determined above, if not, iterate the VCOMP value and recalculate M_1M_2

$$M_1 \times M_2 = 0.538 \times 1.388 \frac{V}{\mu s} = 0.747 \frac{V}{\mu s} \quad (90)$$

The product of M_1 and M_2 is within 1% of the M_1M_2 factor previously calculated:

$$M_1 \times M_2 \cong M_1M_2 \quad (91)$$

$$0.747 \frac{V}{\mu s} \cong 0.751 \frac{V}{\mu s} \quad (92)$$

If more accuracy was desired, iteration results in a VCOMP value of 3.004 V where M_1M_2 and M_1 x M_2 are both equal to 0.751 V/µs.

The non-linear gain variable, M_3, can now be calculated:

$$M_3 = 0 \text{ if } V_{COMP} < 5 \text{ V} \quad (93)$$

$$M_3 = \frac{f_{SW}}{65 kHz} \times \frac{V}{\mu s} \times (0.0166 \times VCOMP - 0.0083) \text{ if } 0.5 \text{ V} < V_{COMP} < 1 \text{ V} \quad (94)$$

$$M_3 = \frac{f_{SW}}{65 kHz} \times \frac{V}{\mu s} \times (0.0572 \times VCOMP^2 - 0.0597 \times VCOMP + 0.0155) \text{ if } 1 \text{ V} < V_{COMP} < 2 \text{ V} \quad (95)$$

$$M_3 = \frac{f_{SW}}{65 kHz} \times \frac{V}{\mu s} \times (0.1148 \times VCOMP^2 - 0.1746 \times VCOMP + 0.0586) \text{ if } 2 \text{ V} < V_{COMP} < 4.5 \text{ V} \quad (96)$$

$$M_3 = \frac{f_{SW}}{65 kHz} \times \frac{V}{\mu s} \times (0.1148 \times VCOMP^2 - 0.1746 \times VCOMP + 0.0586) \text{ if } 4.5 \text{ V} < V_{COMP} < 4.6 \text{ V} \quad (97)$$

$$M_3 = 0 \text{ if } 4.6 \text{ V} < V_{COMP} < 5 \text{ V} \quad (98)$$

In this example, using 3.004 V for VCOMP for a more precise calculation, M_3 calculates to 1.035 V/µs:

$$M_3 = \frac{118 kHz}{65 kHz} \times \frac{V}{\mu s} \times (0.1148 \times 3.004^2 - 0.1746 \times 3.004 + 0.0586) = 1.035 \frac{V}{\mu s} \quad (99)$$

For designs that allow a high inductor ripple current, the current averaging pole, which functions to flatten out the ripple current on the input of the PWM comparator, should be at least decade before the converter switching frequency. Analysis on the completed converter may be needed to determine the ideal compensation pole for the current averaging circuit as too large of a capacitor on ICOMP will add phase lag and increase i_{THD} where as too small of an I_{COMP} capacitor will result in not enough averaging and an unstable current averaging loop. The frequency of the current averaging pole, f_{IAVG}, is chosen to be at approximately 5 kHz for this design as the current ripple factor, ΔI_{RIPPLE}, was chosen at the onset of the design process to be 40%, which is large enough to force DCM operation and result in relatively high inductor ripple current. The required capacitor on ICOMP, C_{ICOMP}, for this is determined using the transconductance gain, g_{mi}, of the internal current amplifier:

$$C_{ICOMP} = \frac{g_{mi} \times M_1}{K_1 2\pi f_{IAVG}} \tag{100}$$

$$C_{ICOMP} = \frac{0.95\,mS \times 0.538}{7 \times 2 \times \pi \times 5\,kHz} = 2330\,pF \tag{101}$$

A standard value 2700-pF capacitor for C_{ICOMP} results in a current averaging pole frequency of 4.314 kHz.

$$f_{IAVG} = \frac{g_{mi} \times M_1}{K_1 \times 2 \times \pi \times 2700\,pF} = 4.314\,kHz \tag{102}$$

The transfer function of the current loop can be plotted:

$$G_{CL}(f) = \frac{K_1 2.5 R_{SENSE} V_{OUT}}{K_{FQ} M_1 M_2 L_{BST}} \times \frac{1}{s(f) + \frac{s(f)^2 K_1 C_{ICOMP}}{g_{mi} \times M_1}} \tag{103}$$

$$G_{CLdB}(f) = 20\log\left(\left|G_{CL}(f)\right|\right) \tag{104}$$

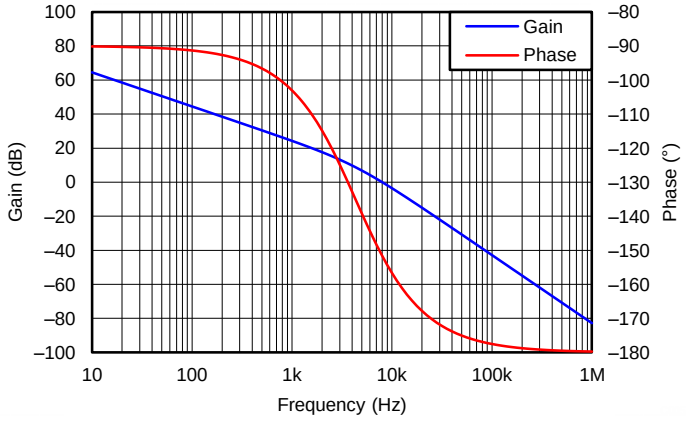


图 32. Bode Plot of the Current Averaging Circuit

The voltage transfer function, $G_{VL(f)}$ contains the product of the voltage feedback gain, G_{FB}, and the gain from the pulse width modulator to the power stage, G_{PWM_PS}, which includes the pulse width modulator to power stage pole, f_{PWM_PS}. The plotted result is shown in 图 32.

$$G_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}}$$

$$G_{FB} = \frac{13\,k\Omega}{1M\Omega + 13\,k\Omega} = 0.013 \tag{105}$$

$$f_{PWM\_PS} = \frac{1}{2\pi \frac{K_1 2.5 R_{SENSE} V_{OUT}^3 C_{OUT}}{K_{FQ} M_1 M_2 V_{IN(nom)}^2}}$$

$$f_{PWM\_PS} = \frac{1}{2\pi \frac{7 \times 2.5 \times 0.032\Omega \times 390V^3 \times 270\mu F}{8.475\mu s \times 0.539 \times 1.392 \frac{V}{\mu s} \times 115\,V^2}} = 1.479Hz \quad (106)$$

$$G_{PWM\_PS}(f) = \frac{\frac{M_3 V_{OUT}}{M_1 M_2 \times 1V}}{1 + \frac{s(f)}{2\pi f_{PWM\_PS}}} \quad (107)$$

$$G_{VL}(f) = G_{FB} G_{PWM\_PS}(f)$$

$$G_{VLdB}(f) = 20\log\left(\left|G_{VL}(f)\right|\right) \quad (108)$$

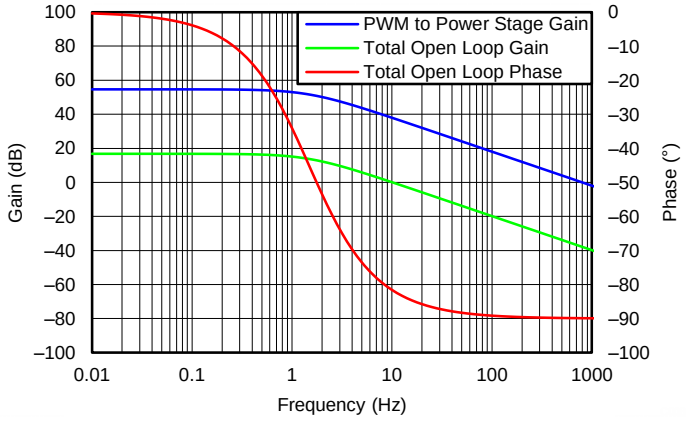


图 33. Bode Plot of the Open Voltage Loop without Error Amplifier

The voltage error amplifier is compensated with a zero, f_{ZERO}, at the f_{PWM_PS} pole and a pole, f_{POLE}, placed at 20 Hz to reject high frequency noise and roll off the gain amplitude. The overall voltage loop crossover, f_V, is desired to be at 10 Hz. The compensation components of the voltage error amplifier are selected accordingly.

$$f_{ZERO} = \frac{1}{2\pi R_{VCOMP} C_{VCOMP}} \quad (109)$$

$$f_{POLE} = \frac{1}{2\pi \frac{R_{VCOMP} C_{VCOMP} C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}}} \quad (110)$$

$$G_{EA}(f) = g_{mv} \left[\frac{1 + s(f) R_{VCOMP} C_{VCOMP}}{\left(C_{VCOMP} + C_{VCOMP\_P}\right) s(f) \left[1 + s(f) \left(\frac{R_{VCOMP} C_{VCOMP} C_{VCOMP\_P}}{C_{VCOMP} + C_{VCOMP\_P}} \right)\right]} \right] \quad (111)$$

From 图 33, the gain of the voltage transfer function at 10 Hz is approximately 0.081 dB. Estimating that the parallel capacitor, C_{VCOMP_P}, is much smaller than the series capacitor, C_{VCOMP}, the unity gain will be at f_V, and the zero will be at f_{PWM_PS}, the series compensation capacitor is determined:

$$f_V = 10Hz \quad (112)$$

$$C_{VCOMP} = \frac{g_{mv} \frac{f_V}{f_{PWM\_PS}}}{10^{\frac{0-G_{VLdB}(f)}{20}} \times 2\pi f_V} \quad (113)$$

$$C_{VCOMP} = \frac{56\,\mu s \times \frac{10\,Hz}{1.479\,Hz}}{10^{\frac{0-0.081dB}{20}} \times 2 \times \pi \times 10\,Hz} = 6.08\,\mu F \quad (114)$$

The capacitor for VCOMP must have a voltage rating that is greater than the absolute maximum voltage rating of the VCOMP pin, which is 7 V. The readily available standard value capacitor that is rated for at least 10 V in the package size that would fit the application was 4.7 µF and this is the value used for C_{VCOMP} in this design example.

R_{VCOMP} is calculated using the actual C_{VCOMP} capacitor value.

$$C_{VCOMP} = 4.7\,\mu F \quad (115)$$

$$R_{VCOMP} = \frac{1}{2\pi f_{ZERO} C_{VCOMP}} \quad (116)$$

$$R_{VCOMP} = \frac{1}{2 \times \pi \times 1.479\,Hz \times 4.7\,\mu F} = 22.89\,k\Omega \quad (117)$$

A 22.6-kΩ resistor is used for R_{VCOMP}.

$$C_{VCOMP\_P} = \frac{C_{VCOMP}}{2\pi f_{POLE} R_{VCOMP} C_{VCOMP} - 1} \quad (118)$$

$$C_{VCOMP\_P} = \frac{4.7\,\mu F}{2 \times \pi \times 20\,Hz \times 22.6k\,k\Omega \times 4.7\,\mu F - 1} = 0.381\mu F \quad (119)$$

A 0.47-µF capacitor is used for C_{VCOMP_P}.

The total closed loop transfer function, G_{VL_total}, contains the combined stages and is plotted in 图 34.

$$G_{VL\_total}(f) = G_{FB}(f) G_{PWM\_PS}(f) G_{EA}(f) \quad (120)$$

$$G_{VL\_totaldB}(f) = 20\log\left(\left|G_{VL\_total}(f)\right|\right) \quad (121)$$

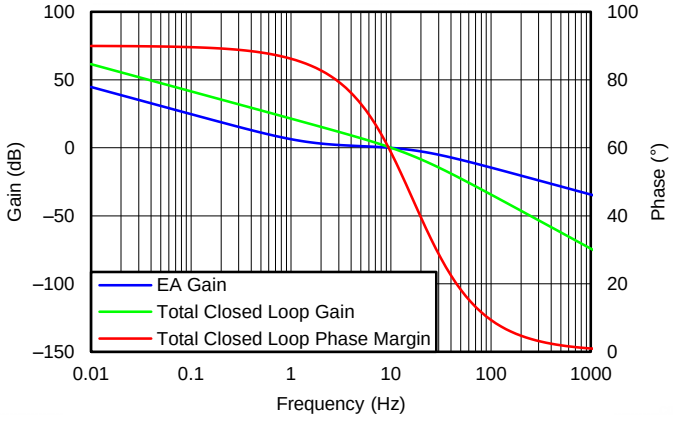


图 34. Closed Loop Voltage Bode Plot

9.2.3 Application Curve

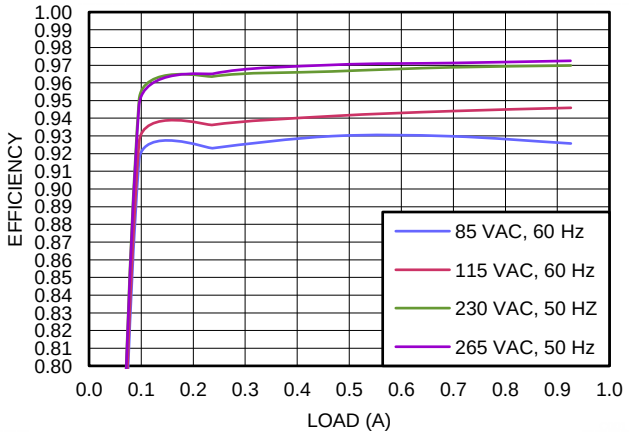


图 35. UCC28180EVM-573 Efficiency (As a Function of Line Voltage and Load Current)

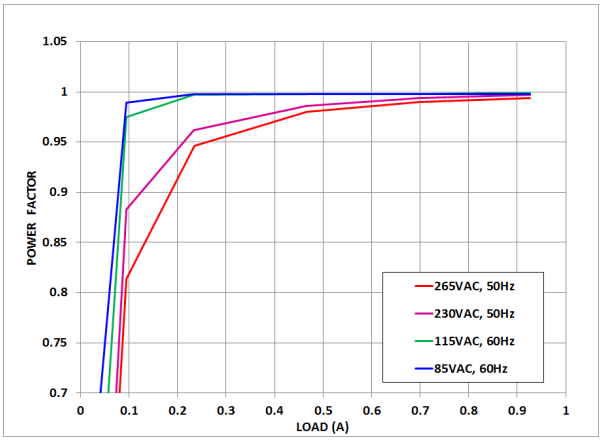


图 36. UCC28180EVM-573 Power Factor (As a Function of Line Voltage and Load Current)

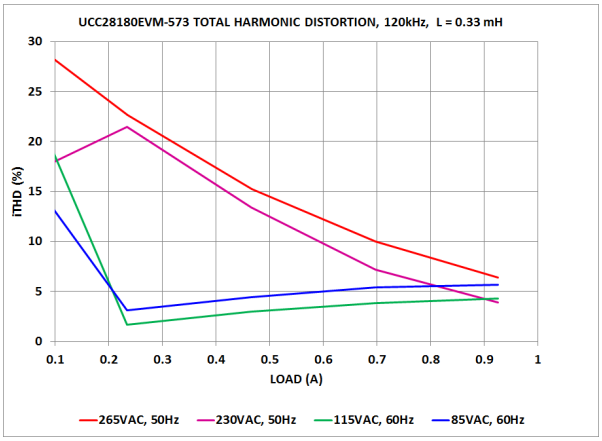


图 37. UCC28180EVM-573 Total Harmonic Distortion (As a Function of Line Voltage and Load Current)

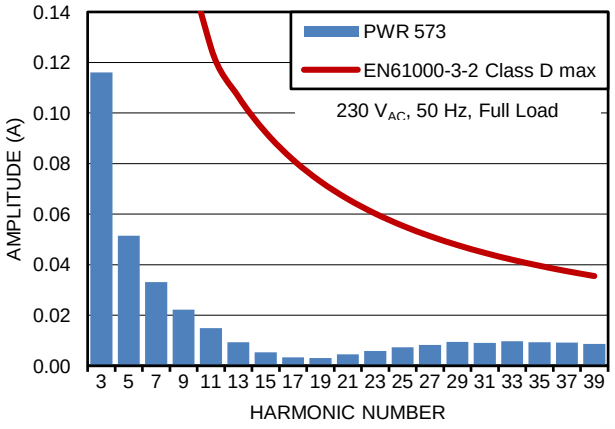


图 38. UCC28180EVM-573 Current Harmonics, (230-V_{AC}, 50-Hz Input, Full Load, Without the Fundamental)

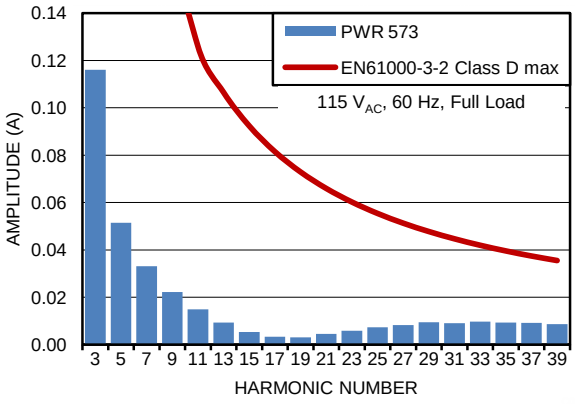


图 39. UCC28180EVM-573 Current Harmonics, (115-V_{AC}, 60-Hz Input, Full Load, Without the Fundamental)

10 Power Supply Recommendations

10.1 Bias Supply

The UCC28180 operates from an external bias supply. It is recommended that the device be powered from a regulated auxiliary supply. (This device is not intended to be used from a *bootstrap* bias supply. A *bootstrap* bias supply is fed from the input high voltage through a resistor with sufficient capacitance on VCC to hold up the voltage on VCC until current can be supplied from a bias winding on the boost inductor. For that reason, the minimal hysteresis on VCC would require an unreasonable value of hold-up capacitance.)

During normal operation, when the output is regulated, current drawn by the device includes the nominal run current plus the current supplied to the gate of the external boost switch. Decoupling of the bias supply must take switching current into account in order to keep ripple voltage on VCC to a minimum. A ceramic capacitor of 0.1-µF minimum value from VCC to GND with short, wide traces is recommended.

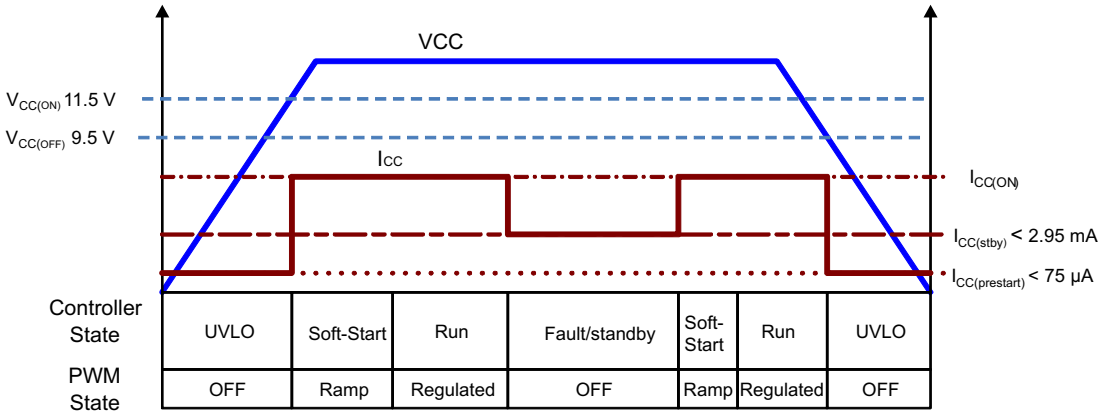


图 40. Device Supply States

The device's bias operates in several states. During startup, VCC Under-Voltage LockOut (UVLO) sets the minimum operational DC input voltage of the controller. There are two UVLO thresholds. When the UVLO turn-on threshold is exceeded, the PFC controller turns ON. If the VCC voltage falls below the UVLO turn-off threshold, the PFC controller turns off. During UVLO, current drawn by the device is minimal. After the device turns on, Soft Start (SS) is initiated and the boost inductor current is ramped up in a controlled manner to reduce the stress on the external components and avoids output voltage overshoot. During soft start and after the output is in regulation, the device draws its normal run current. If any of several fault conditions are encountered or if the device is put in standby with an external signal, the device draws a reduced standby current.

11 Layout

11.1 Layout Guidelines

As with all PWM controllers, the effectiveness of the filter capacitors on the signal pins depends upon the integrity of the ground return. Separating the high di/dt induced noise on the power ground from the low current quiet signal ground is required for adequate noise immunity. Even with a signal layer PCB design, the pin out of the UCC28180 is ideally suited to minimize noise on the small signal traces. As shown in 图 41, the capacitors on VSENSE, VCOMP, ISENSE, ICOMP, and FREQ (if used) must be all be returned directly to the portion of the ground plane that is the quiet signal GND and not in high-current return path of the converter, shown as power GND. The trace from the FREQ pin to the frequency programming resistor should be as short as possible. It is recommended that the compensation components on ICOMP and VCOMP are located as close as possible to the UCC28180. Placement of these components should take precedence, paying close attention to keeping their traces away from high noise areas. The bypass capacitors on VCC must be located physically close the VCC and GND pins of the UCC28180 but should not be in the immediate path of the signal return.

Layout Guidelines (接下页)

Other layout considerations should include keeping the switch node as short as possible, with a wide trace to reduce induced ringing caused by parasitic inductance. Every effort should be made to avoid noise from the switch node from corrupting the small signal traces with adequate clearance and ground shielding. As some compromises must be made due to limitation of PCB layers or space constraints, traces that must be made long, such as the signal from the current sense resistor shown in 图 41, should be as wide as possible, avoid long narrow traces.

表 2. Layout Component Description for 图 41

LAYOUT COMPONENTS	
REFERENCE DESIGNATOR	**FUNCTION**
U1	Controller, UCC28180
Q1	Main switch
D2	Boost diode
R5	RGATE
R7	Pull-down resistor on GATE
D1	Turn-off diode on GATE
D4	ISENSE pin diode
C11, C12	VCC bypass capacitors
C7	ICOMP compensation, C_{ICOMP}
R1, C6	Placeholders for additional ICOMP compensation, if needed
C8	ISENSE filter, C_{ISENSE}
R2	ISENSE inrush current limiting resistor, R_{ISENSE}
R3	Frequency programming resistor, R_{FREQ}
C9	Placeholder for FREQ filter, if needed
R6, C13, C14	VCOMP compensation components, R_{VCOMP}, C_{VCOMP_P}, C_{VCOMP}
C15	VSENSE filter, C_{VSENSE}
R11, R12	R_{FB1} on VSENSE
R13	R_{FB2} on VSENSE

11.2 Layout Example

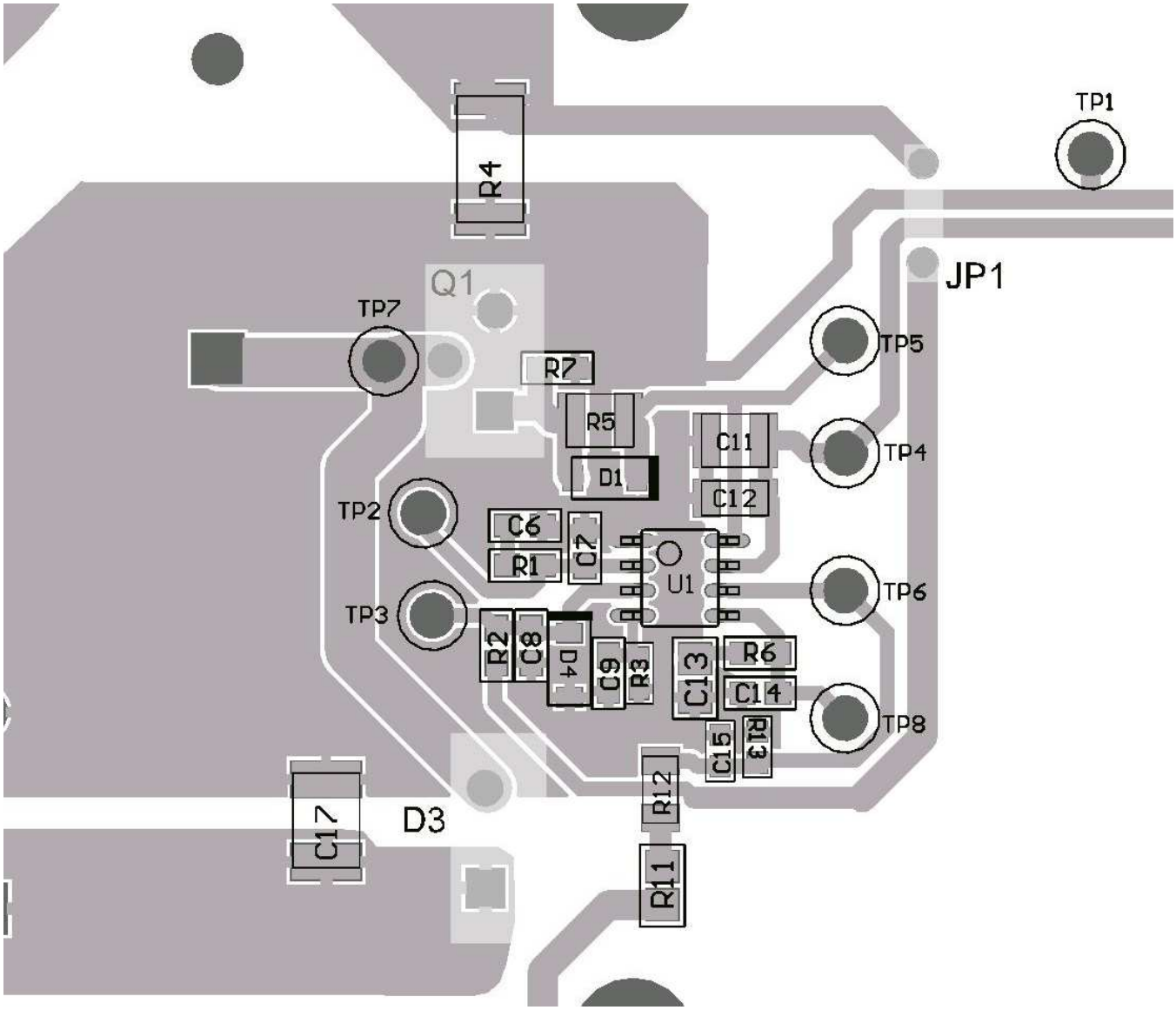


图 41. Recommended Layout for UCC28180

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

这些参考资料、附加设计工具以及附加参考资料的链接（包括设计软件和模型）均可在 http://www.power.ti.com 网站的“技术文档”下找到。

- 用户指南，*《使用 UCC28180EVM-573 360W 功率因数校正》*，SLUUAT3
- 设计电子表格，*《UCC28180 设计计算器》*，SLUC506

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28180D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28180	Samples
UCC28180DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U28180	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

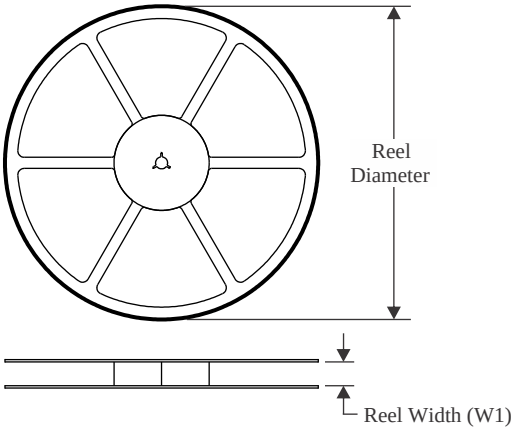
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

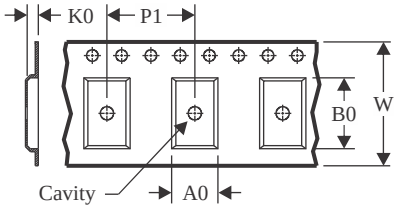
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

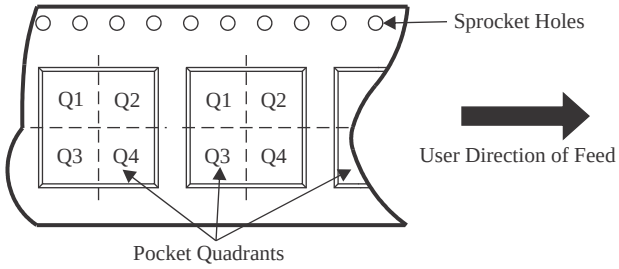


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

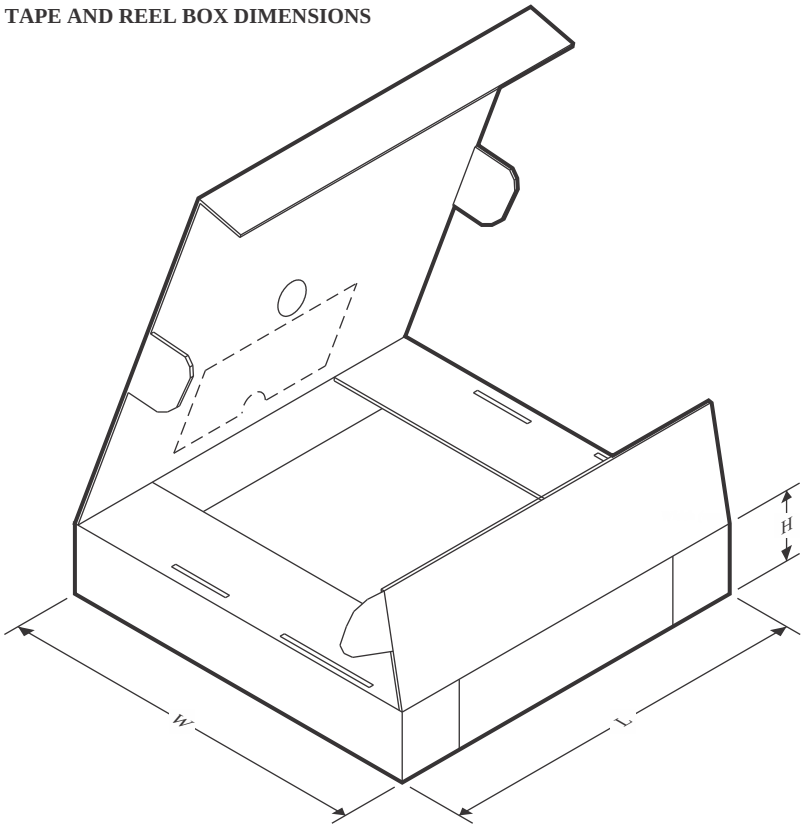
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28180DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

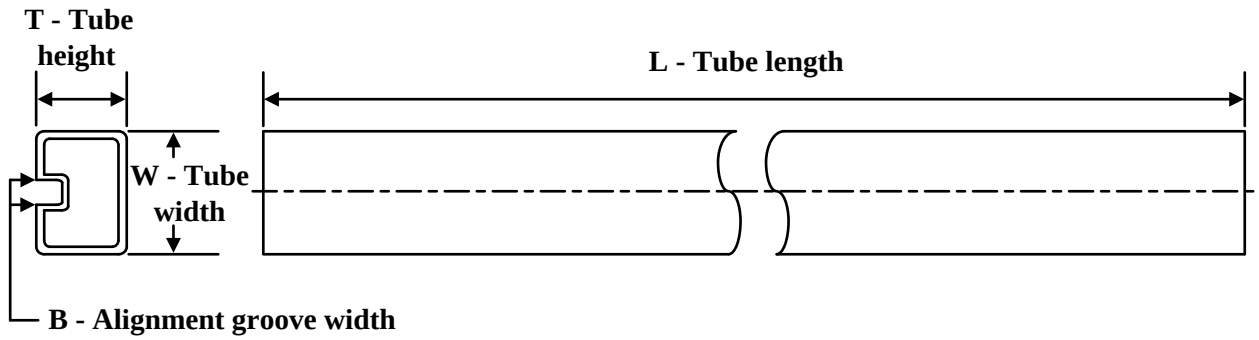
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

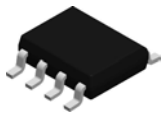
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28180DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC28180D	D	SOIC	8	75	507	8	3940	4.32

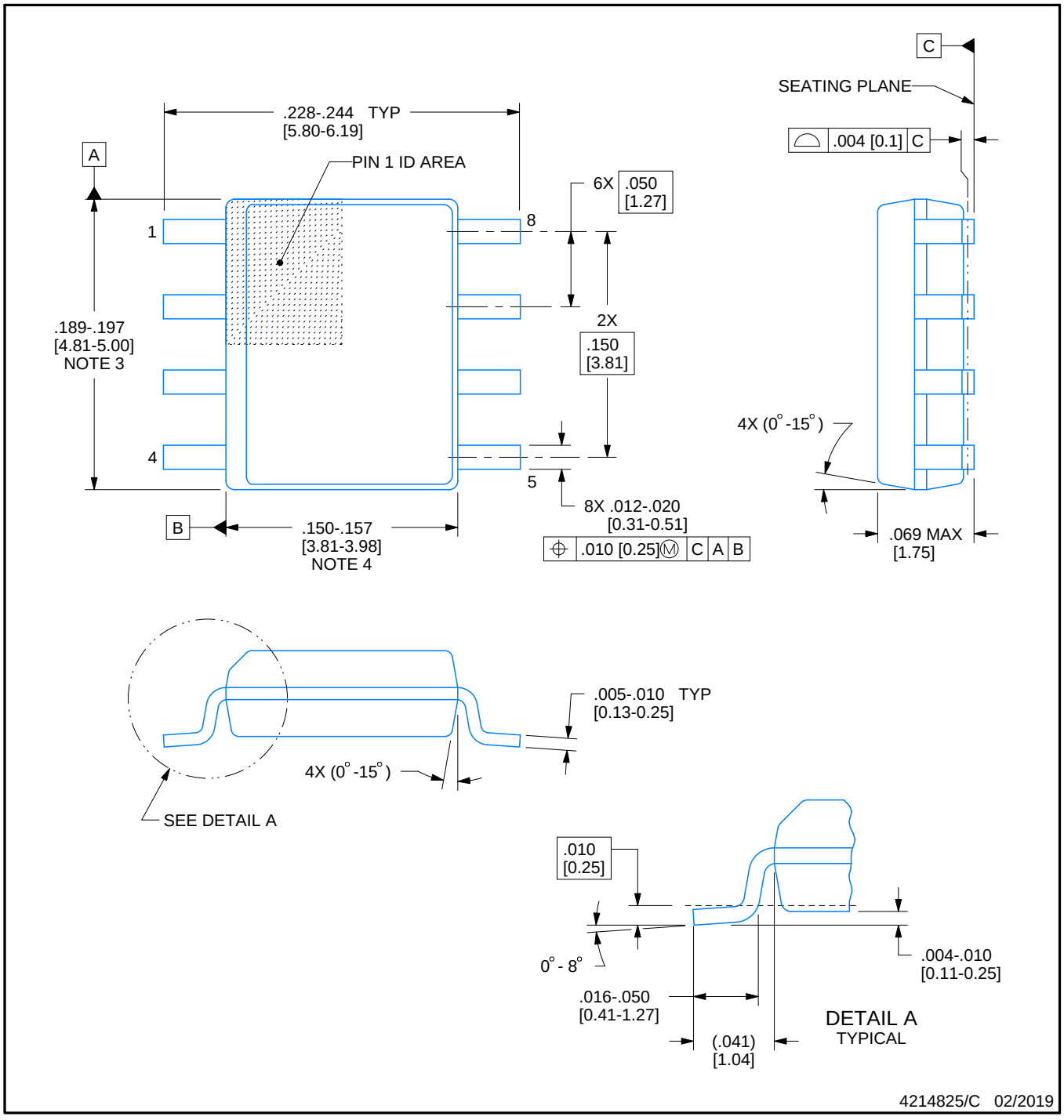


PACKAGE OUTLINE

D0008A

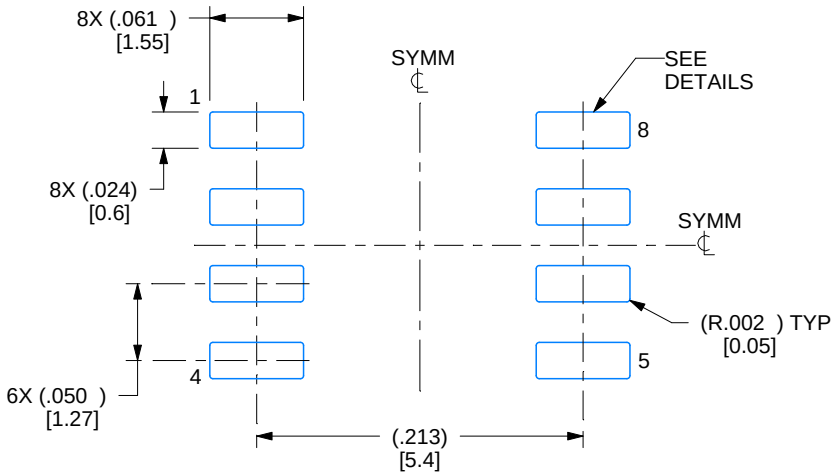
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

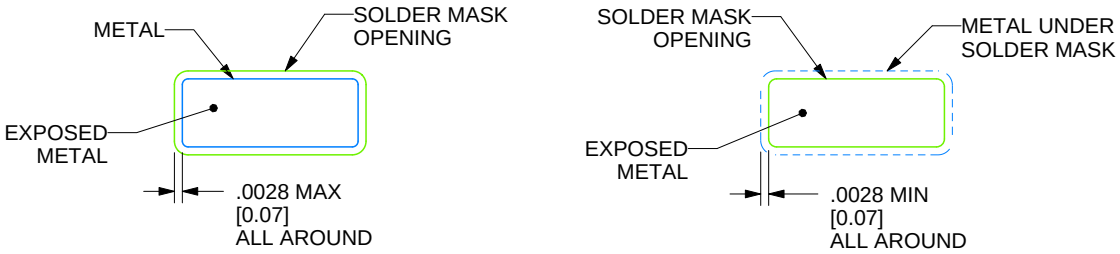


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

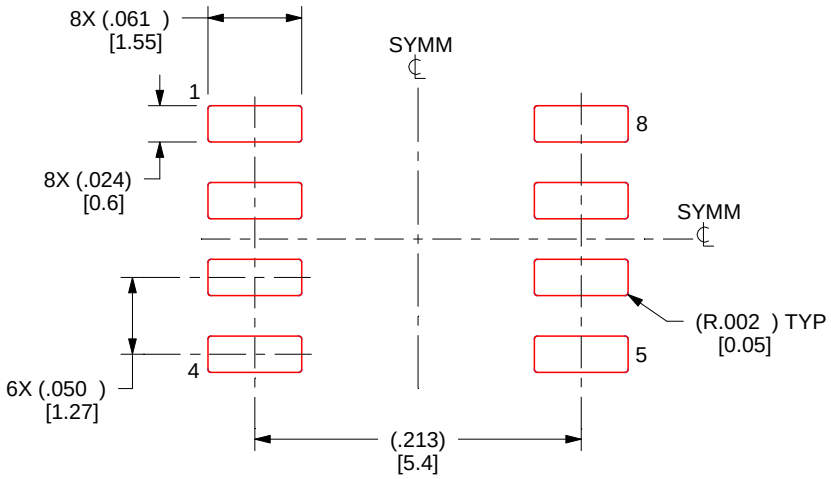
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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