

## MM74HC4020 • MM74HC4040 14-Stage Binary Counter • 12-Stage Binary Counter

### General Description

The MM74HC4020, MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing advanced silicon-gate CMOS technology to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The MM74HC4020 is a 14 stage counter and the MM74HC4040 is a 12-stage counter. Both devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

These devices are pin equivalent to the CD4020 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to  $V_{CC}$  and ground.

### Features

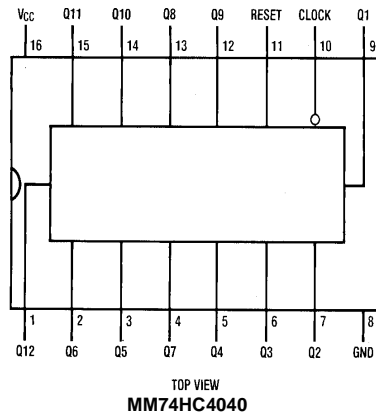
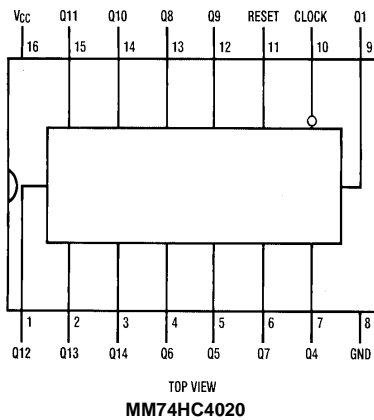
- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1  $\mu$ A maximum
- Low quiescent current: 80  $\mu$ A maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

### Ordering Code:

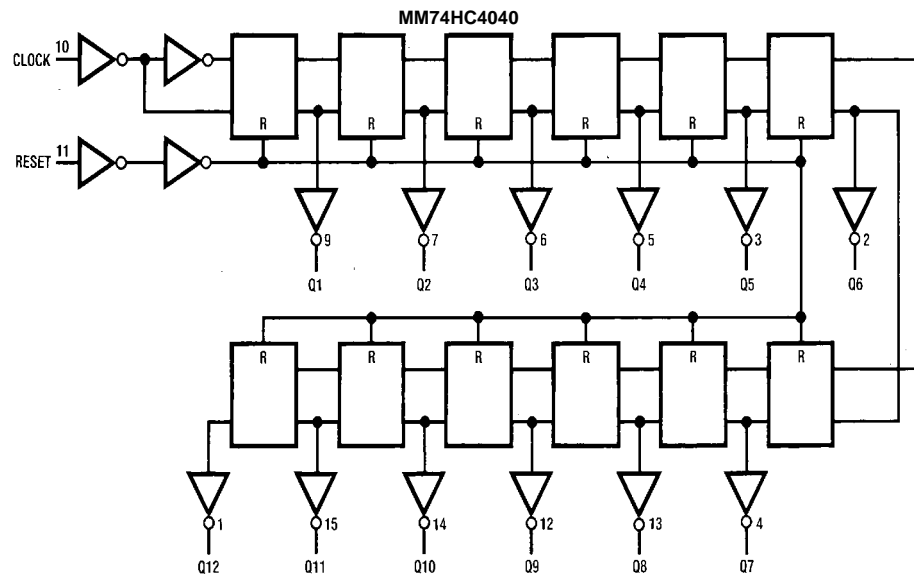
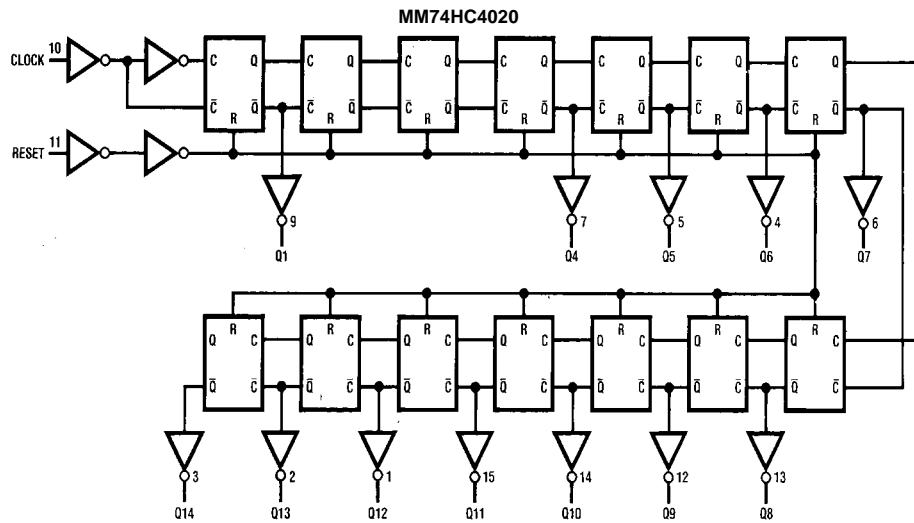
Order Number	Package Number	Package Description
MM74HC4020M (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4020SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4020N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
MM74HC4040M (Note 1)	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC4040SJ (Note 1)	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC4040MTC (Note 1)	MTC-16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC4040N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

**Note 1:** Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagrams



Logic Diagrams



**Absolute Maximum Ratings**(Note 2)

(Note 3)

Supply Voltage ( $V_{CC}$ )	-0.5 to +7.0V
DC Input Voltage ( $V_{IN}$ )	-1.5 to $V_{CC} + 1.5V$
DC Output Voltage ( $V_{OUT}$ )	-0.5 to $V_{CC} + 0.5V$
Clamp Diode Current ( $I_{CD}$ )	$\pm 20$ mA
DC Output Current, per pin ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )	$\pm 50$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
(Note 4)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering 10 seconds)	260°C

**Recommended Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	2	6	V
DC Input or Output Voltage ( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	-40	+85	°C
Input Rise or Fall Times ( $t_r, t_f$ )			
$V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

**Note 2:** Maximum Ratings are those values beyond which damage to the device may occur.

**Note 3:** Unless otherwise specified all voltages are referenced to ground.

**Note 4:** Power Dissipation temperature derating — plastic "N" package: -12 mW/°C from 65°C to 85°C.

**DC Electrical Characteristics** (Note 5)

Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$			$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits				
$V_{IH}$	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V	
			4.5V		3.15	3.15	3.15		
			6.0V		4.2	4.2	4.2		
$V_{IL}$	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V	
			4.5V		1.35	1.35	1.35		
			6.0V		1.8	1.8	1.8		
$V_{OH}$	Minimum HIGH Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4		
			6.0V	6.0	5.9	5.9	5.9		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	4.2	3.98	3.84	3.7		
			6.0V	5.7	5.48	5.34	5.2		
$V_{OL}$	Maximum LOW Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 20 \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1		
			6.0V	0	0.1	0.1	0.1		
		$V_{IN} = V_{IH}$ or $V_{IL}$ $ I_{OUT}  \leq 4.0$ mA $ I_{OUT}  \leq 5.2$ mA	4.5V	0.2	.26	0.33	0.4		
			6.0V	0.2	.26	0.33	0.4		
$I_{IN}$	Maximum Input Current	$V_{IN} = V_{CC}$ or GND	6.0V		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu A$	
$I_{CC}$	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$	6.0V		8.0	80	160	$\mu A$	

**Note 5:** For a power supply of  $5V \pm 10\%$  the worst case output voltages ( $V_{OH}$ , and  $V_{OL}$ ) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case  $V_{IH}$  and  $V_{IL}$  occur at  $V_{CC} = 5.5V$  and 4.5V respectively. (The  $V_{IH}$  value at 5.5V is 3.85V.) The worst case leakage current ( $I_{IN}$ ,  $I_{CC}$ , and  $I_{OZ}$ ) occur for CMOS at the higher voltage and so the 6.0V values should be used.

**AC Electrical Characteristics** $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ ,  $C_L = 15$  pF,  $t_r = t_f = 6$  ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
$f_{MAX}$	Maximum Operating Frequency		50	30	MHz
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Clock to Q	(Note 6)	17	35	ns
$t_{PHL}$	Maximum Propagation Delay Reset to any Q		16	40	ns
$t_{REM}$	Minimum Reset Removal Time		10	20	ns
$t_W$	Minimum Pulse Width		10	16	ns

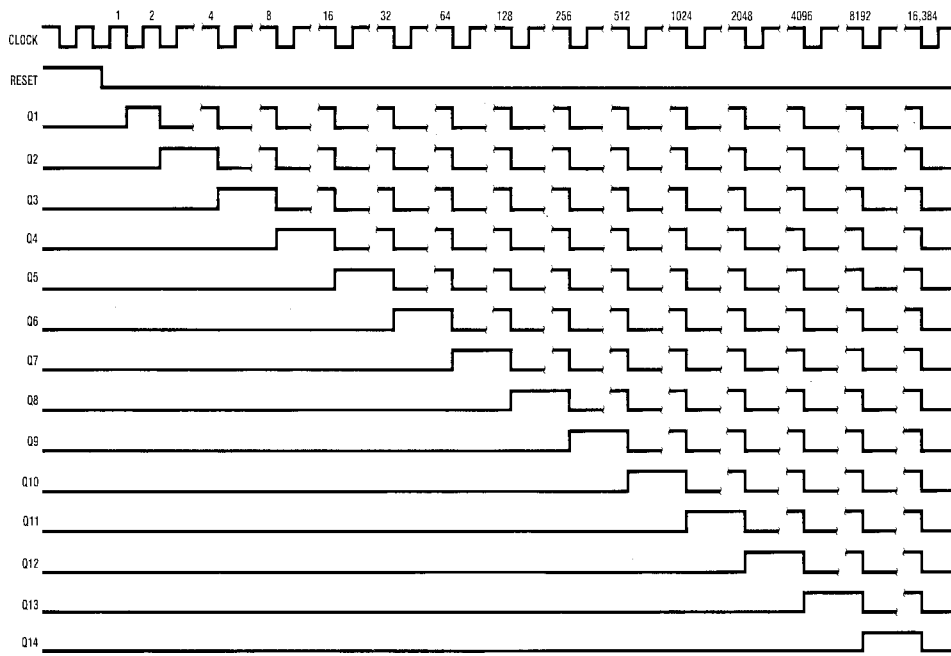
**Note 6:** Typical Propagation delay time to any output can be calculated using:  $t_p = 17 + 12(N-1)$  ns; where N is the number of the output,  $Q_W$ , at  $V_{CC} = 5V$ .

**AC Electrical Characteristics** $V_{CC} = 2.0V$  to  $6.0V$ ,  $C_L = 50$  pF,  $t_r = t_f = 6$  ns (unless otherwise specified)

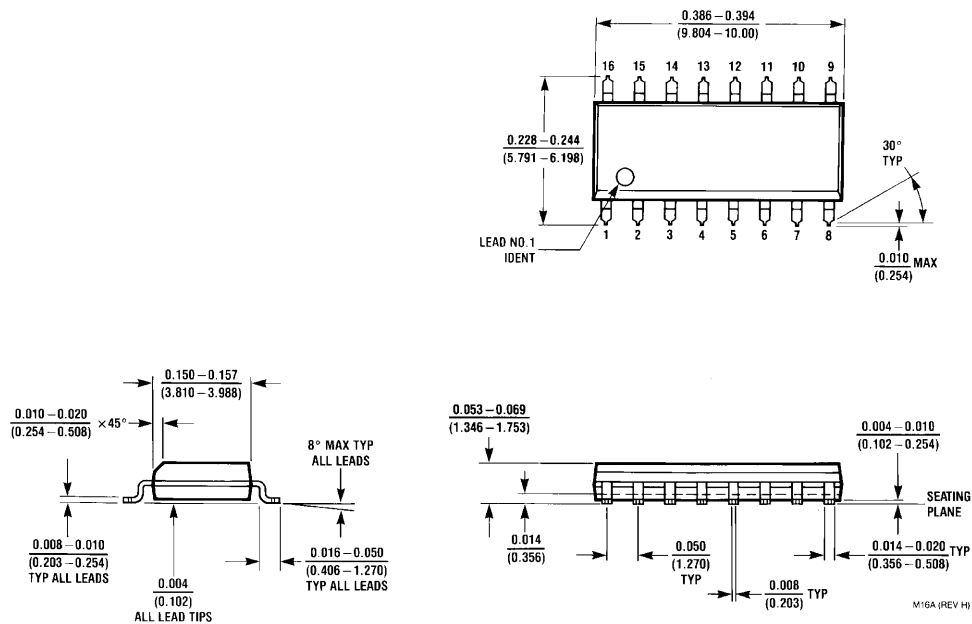
Symbol	Parameter	Conditions	$V_{CC}$	$T_A = 25^\circ C$		$T_A = -40$ to $85^\circ C$	$T_A = -55$ to $125^\circ C$	Units
				Typ	Guaranteed Limits			
$f_{MAX}$	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	
			6.0V	50	35	28	24	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Clock to $Q_1$		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	
			6.0V	18	36	45	53	
$t_{PHL}$ , $t_{PLH}$	Maximum Propagation Delay Between Stages from $Q_n$ to $Q_{n+1}$		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	
			6.0V	15	21	26	31	
$t_{PHL}$	Maximum Propagation Delay Reset to any Q (4020 and 4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	
			6.0V	20	41	51	61	
$t_{REM}$	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	
			6.0V		16	21	25	
$t_W$	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	
			6.0V		14	18	20	
$t_{TLH}$ , $t_{THL}$	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	
			6.0V	9	13	16	19	
$t_r$ , $t_f$	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	
					400	400	400	
$C_{PD}$	Power Dissipation Capacitance (Note 7)	(per package)		55				pF
$C_{IN}$	Maximum Input Capacitance			5	10	10	10	pF

**Note 7:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

### Timing Diagram

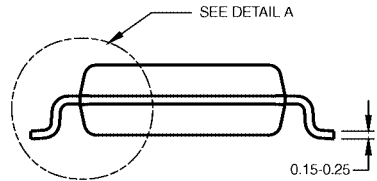
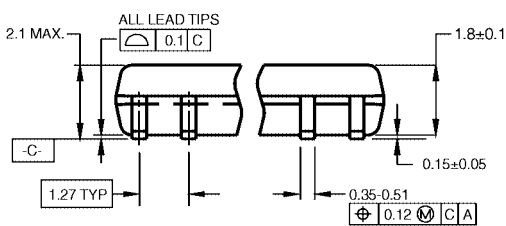


**Physical Dimensions** inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow  
Package Number M16A**

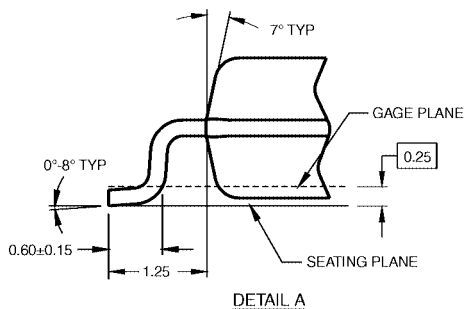
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

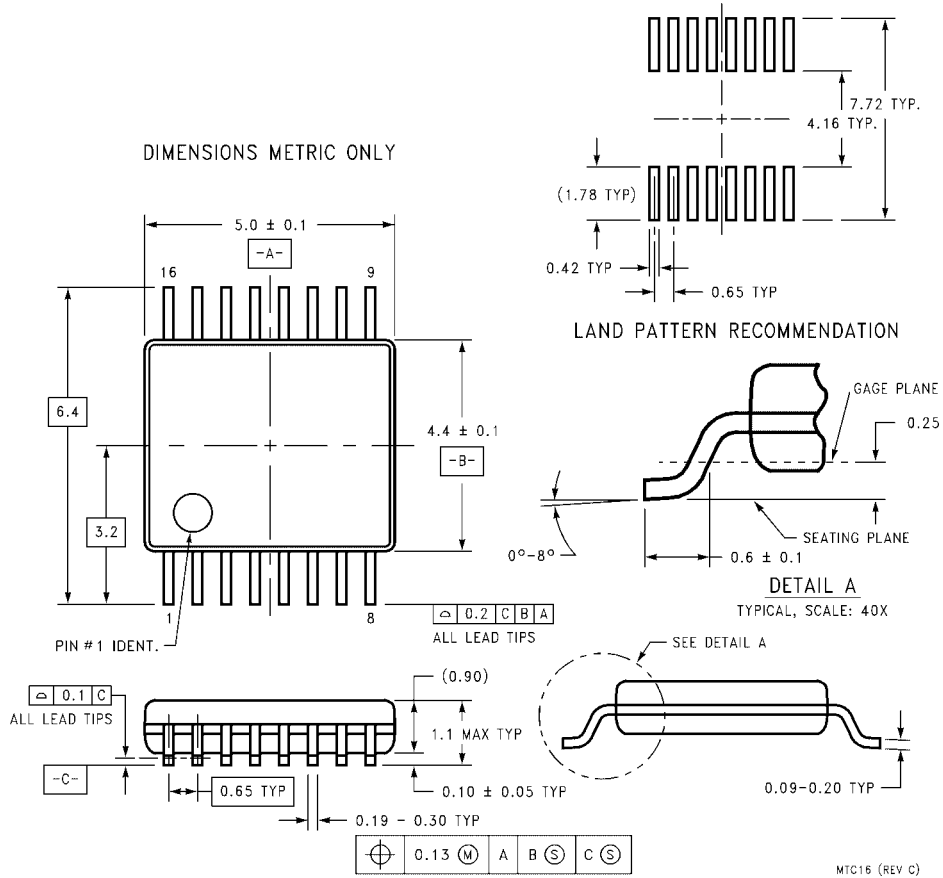
- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
 Package Number M16D**

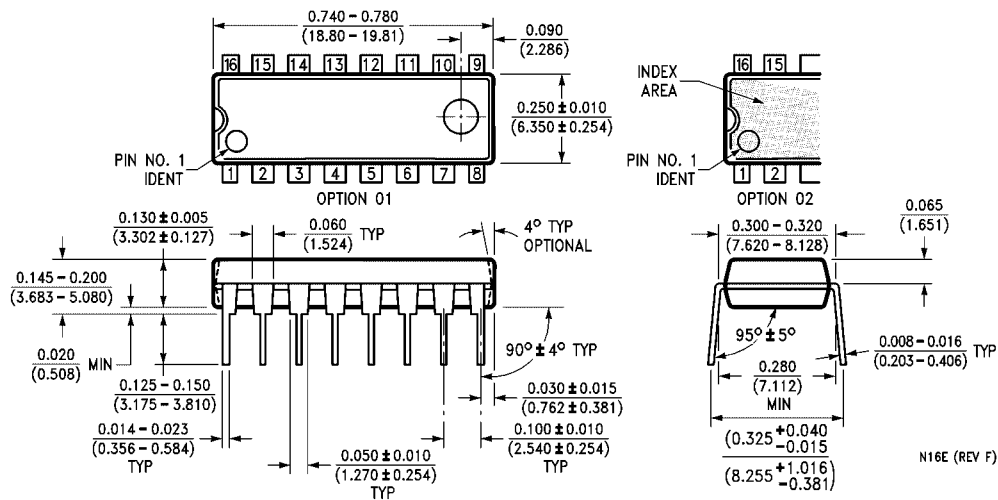
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC16**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)