TEXAS INSTRUMENTS

SN55451B, SN55452B, SN55453B, SN55454B
SN75451B, SN75452B, SN75453B, SN75454B

SLRS021D – DECEMBER 1967 – REVISED JANUARY 2017

SN5545xB, SN7545xB Dual-Peripheral Drivers for High-Current, High-Speed Switching

1 Features

- Characterized for Use to 300 mA
- High-Voltage Outputs up to 30 V
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Open-Collector Outputs
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages

2 Applications

- High-Speed Logic Buffers
- Power Drivers
- Lamp Drivers
- LED Drivers
- Line Drivers
- Memory Drivers

3 Description

The SN5545xB and SN7545xB devices are dual-peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design.

The SNx5451B, SNx5452B, SNx5453B, and SNx5454B devices are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

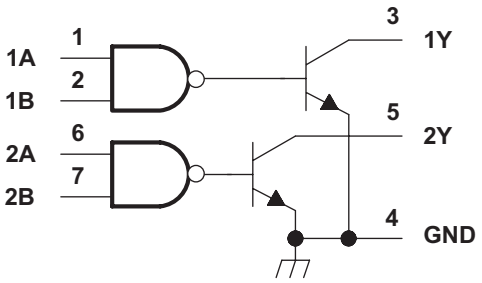
The SN5545xB drivers are characterized for operation over the full military range of –55°C to 125°C. The SN7545xB drivers are characterized for operation from 0°C to 70°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN7545xBP	PDIP (8)	9.81 mm × 6.35 mm
SN7545xBD	SOIC (8)	4.90 mm × 3.90 mm
SN7545xBPS	SO (8)	6.20 mm x 5.30 mm
SN5545xBJG	CDIP (8)	9.60 mm × 6.67 mm
SN5545xBFK	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN75451B Logic Diagram



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4 Revision History

Changes from Revision C (May 2016) to Revision D **Page**

- Replaced image *SN75451B Logic Diagram* ... 1

Changes from Revision B (January 1999) to Revision C **Page**

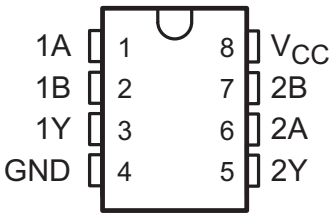
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Device Comparison Table

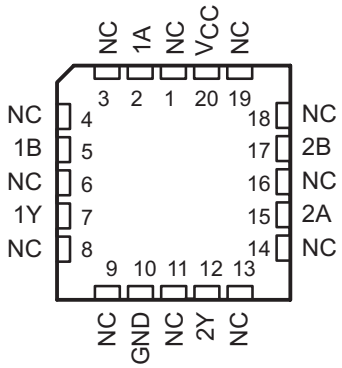
DEVICE	LOGIC OF COMPLETE CIRCUIT	OPERATING FREE AIR TEMPERATURE RANGE
SN55451B	AND	–55°C to 125°C
SN55452B	NAND	–55°C to 125°C
SN55453B	OR	–55°C to 125°C
SN55454B	NOR	–55°C to 125°C
SN75451B	AND	0°C to 70°C
SN75452B	NAND	0°C to 70°C
SN75453B	OR	0°C to 70°C
SN75454B	NOR	0°C to 70°C

6 Pin Configuration and Functions

JG, D, P, or PS Package
8-Pin CDIP, SOIC, PDIP, or SO
Top View



FK Package
20-Pin LCCC
Top View



NC – No internal connection

Pin Functions

PIN			I/O	DESCRIPTION
NAME	CDIP, SOIC, PDIP, SO	LCCC		
1A	1	2	I	Channel 1 Logic Input A
1B	2	5	I	Channel 1 Logic Input B
1Y	3	7	O	Channel 1 Driver
2A	6	15	I	Channel 2 Logic Input A
2B	7	17	I	Channel 2 Logic Input B
2Y	5	12	O	Channel 2 Driver
GND	4	10	—	Ground
NC	—	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	No Internal Connection
VCC	8	20	—	Supply Voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage, (see (2))			7	V
V_I	Input voltage			5.5	V
	Inter-emitter voltage (see Note (3))			5.5	V
V_O	Off-state output voltage			30	V
I_{OK}	Continuous collector or output current, (see Note (4))			400	mA
	Peak collector or output current, II (tw ≤ 10 ms, duty cycle ≤ 50%, see Note (5))			500	mA
	Continuous total power dissipation		See *Dissipation Ratings*		
T_A	Operating free-air temperature	SN5545xB	–55	125	°C
		SN7545xB	0	70	
	Case temperature for 60 seconds	SN5545xB FK package		260	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	SN5545xB JG package		100	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	SN7545xB D or P package		260	°C
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to network GND, unless otherwise specified.
(3) This is the voltage between two emitters of a multiple-emitter transistor.
(4) This value applies when the base-emitter resistance (RBE) is equal to or less than 500 Ω.
(5) Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	SN5545xB	4.5	5	5.5	V
		SN7545xB	4.75	5	5.25	
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating free-air temperature	SN5545xB	–50		125	°C
		SN7545xB	0		70	

7.3 Thermal Information

THERMAL METRIC(1)		SN7545xB			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.2	63.7	119.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.4	53.6	71.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.4	40.8	68.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.2	31.1	31.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.0	40.8	67.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = – 12 mA			–1.2	–1.5	V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, IOL = 100 mA	SN5545xB		0.25	0.5	V
			SN7545xB		0.25	0.4	
		V_{CC} = MIN, V_{IL} = 0.8 V, IOL = 300 mA	SN5545xB		0.5	0.8	
			SN7545xB		0.5	0.7	
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, VOH = 30 V	SN5545xB			300	µA
			SN7545xB			100	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			–1	–1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V	SNx5451B		7	11	mA
			SNx5453B		8	11	
		V_{CC} = MAX, V_I = 0 V	SNx5452B		11	14	
			SNx5454B		13	17	
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0 V	SNx5451B		52	65	mA
			SNx5453B		54	68	
		V_{CC} = MAX, V_I = 5 V	SNx5452B		56	71	
			SNx5454B		61	79	

7.5 Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

over operating free-air temperature range (unless otherwise noted)

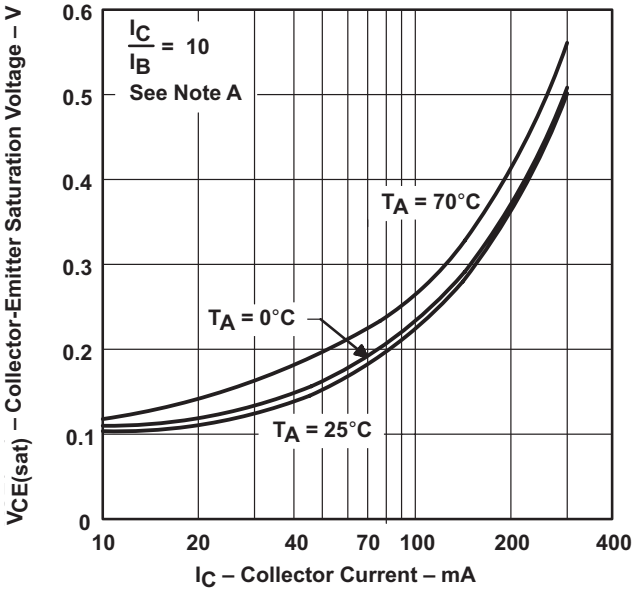
PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 2	SNx5451B, SNx5453B		18	25	ns
			SNx5452B		26	35	
			SNx5454B		27	35	
t_{PHL}	Propagation delay time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 2	SNx5451B, SNx5453B		18	25	
			SNx5452B, SNx5454B		24	35	
tTLH	Transition time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 2			5	8	
t_{THL}	Transition time, high-to-low-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, L See Figure 2			7	12	
V_{OH}	High level output voltage after switching	VS = 20 V, IO 9 300 mA, See Figure 2	SN5545xB	V_S – 6.5			mV
			SN7545xB	V_S – 6.5			

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V, T_A = 25°C.

7.6 Dissipation Ratings

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 125°C POWER RATING
D	725 mW	5.8 mW/°C	464	—
FK	1375 mW	11.0 mW/°C	880	275 mW
JG	1050 mW	8.4 mW/°C	672	210 mW
P	1000 mW	8.0 mW/°C	640	—

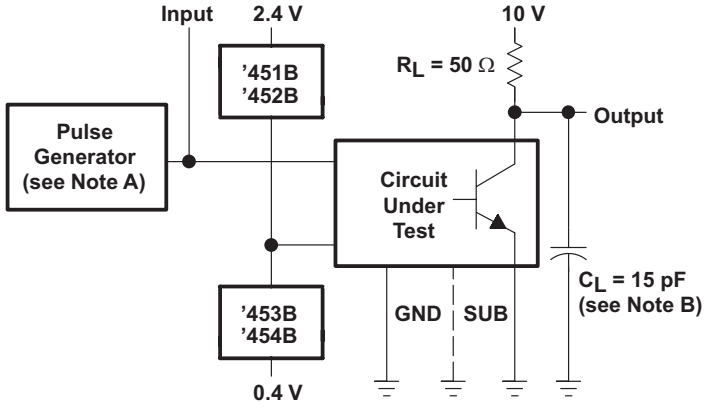
7.7 Typical Characteristics



NOTE A: These parameters must be measured using pulse techniques, t_W = 300 μs, duty cycle ≤ 2%.

Figure 1. Transistor Collector-Emitter Saturation Voltage vs Collector Current

8 Parameter Measurement Information

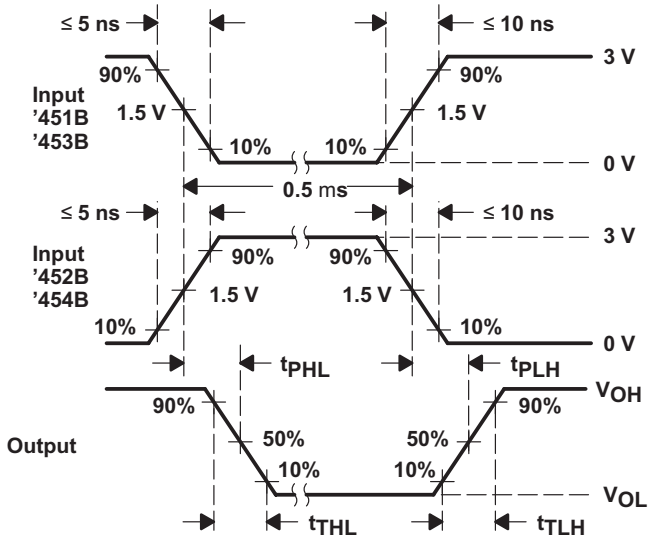


A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω.

B. CL includes probe and jig capacitance.

Figure 2. Test Circuit, Complete Drivers

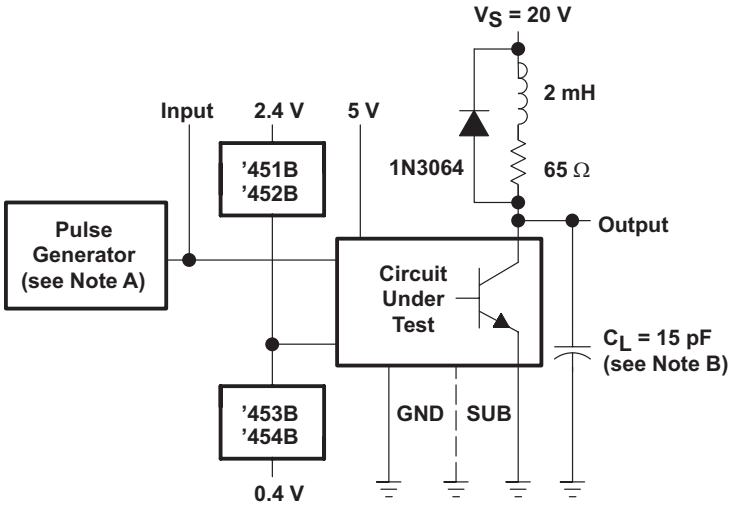
Parameter Measurement Information (continued)



A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, ZO = 50 Ω.

B. CL includes probe and jig capacitance.

Figure 3. Waveforms, Complete Drivers

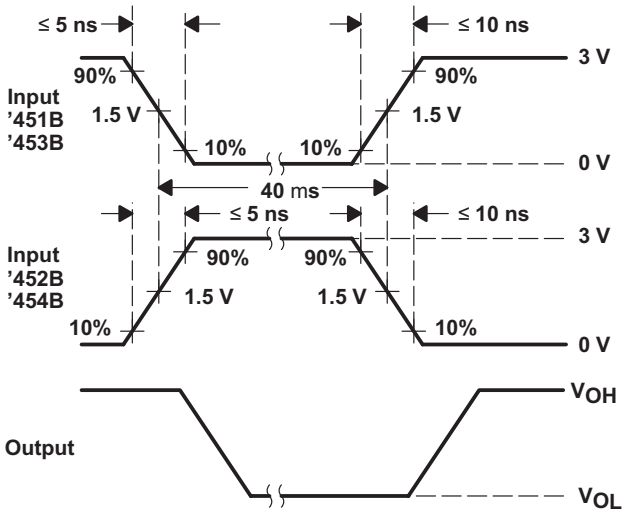


A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, ZO = 50 Ω.

B. CL includes probe and jig capacitance.

Figure 4. Test Circuit for Latch-Up Test of Complete Drivers

Parameter Measurement Information (continued)



A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, ZO = 50 Ω.

B. CL includes probe and jig capacitance.

Figure 5. Voltage Waveforms for Latch-Up Test of Complete Drivers

9 Detailed Description

9.1 Overview

The SN7545xB and SN5545xB devices provide dual-output drivers with AND, NAND, NOR, or OR logic inputs. If each logic input is set to the appropriate voltage level, then the output driver will turn on, pulling the driver to ground and allowing current to flow.

9.2 Functional Block Diagrams

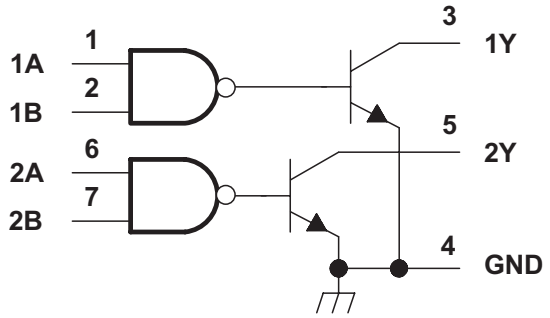


Figure 6. SNx5451B Logic Diagram (Positive Logic)

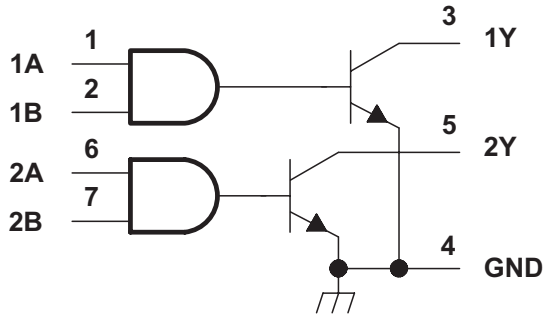


Figure 7. SNx5452B Logic Diagram (Positive Logic)

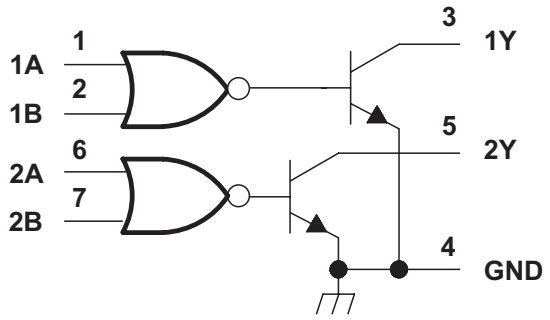


Figure 8. SNx5453B Logic Diagram (Positive Logic)

Functional Block Diagrams (continued)

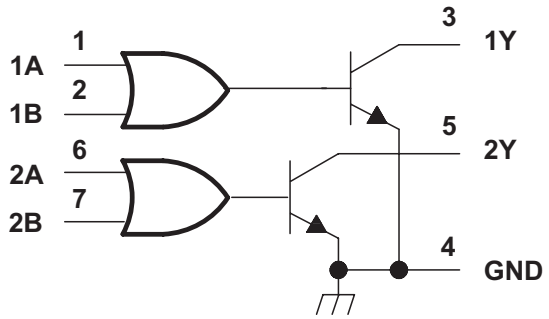


Figure 9. SNx5454B Logic Diagram (Positive Logic)

9.3 Feature Description

The SNx5451B devices allow for high current driving up to 300 mA. This family of devices have AND, NAND, OR, or NOR input logic gates to allow for a wide variety of applications. The SN7545xB devices are rated for a commercial temperature range of 0°C to 70°C, and the SN5545xB devices are rated for a military temperature range of –65°C to 125°C.

9.4 Device Functional Modes

Table 1, Table 2, Table 3, and Table 4 list the functional modes of the SNx545xB.

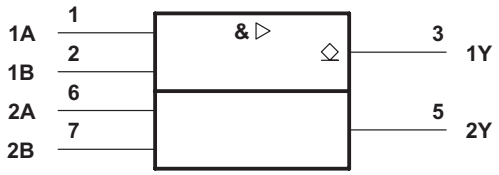


Figure 10. SNx5451B Logic Symbol

Table 1. SNx5451B Function Table

A	B	Y (1)
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

(1) Positive logic: Y = AB or NOT($\overline{A}$ + $\overline{B}$)

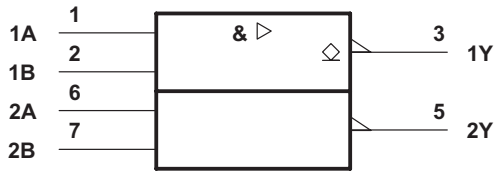


Figure 11. SNx5452B Logic Symbol

Table 2. SNx5452B Function Table

A	B	Y (1)
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

(1) Positive logic: $Y = \overline{AB}$ or $\overline{A} + \overline{B}$

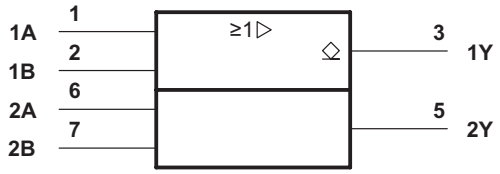


Figure 12. SNx5453B Logic Symbol

Table 3. SNx5453B Function Table

A	B	Y (1)
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

(1) Positive logic: $Y = AB$ or $NOT(\overline{A} + \overline{B})$

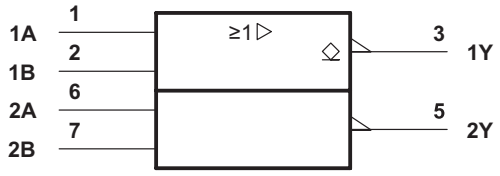


Figure 13. SNx5454B Logic Symbol

Table 4. SNx5454B Function Table

A	B	Y (1)
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

(1) Positive logic: $Y = \overline{A+B}$ or $\overline{A}\ \overline{B}$

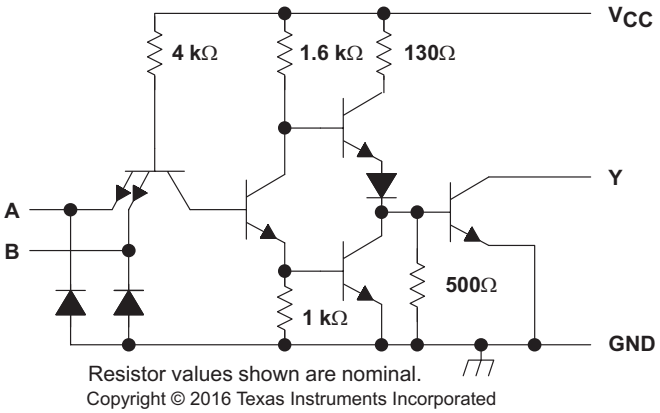


Figure 14. SNx5451B Schematic (Each Driver)

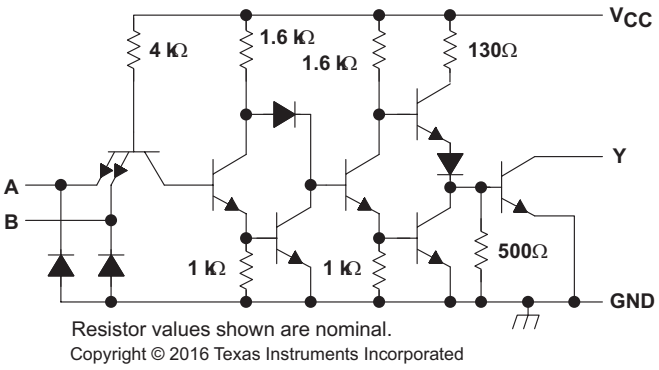


Figure 15. SNx5452B Schematic (Each Driver)

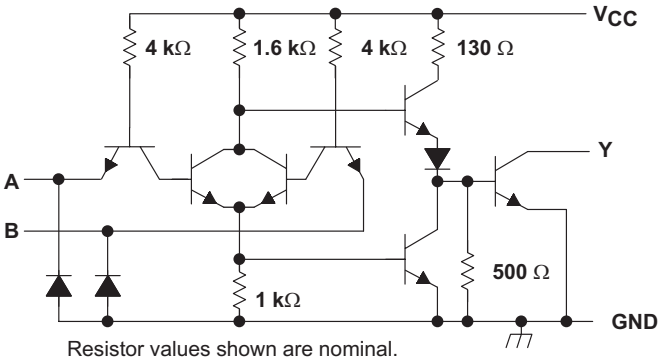


Figure 16. SNx5453B Schematic (Each Driver)

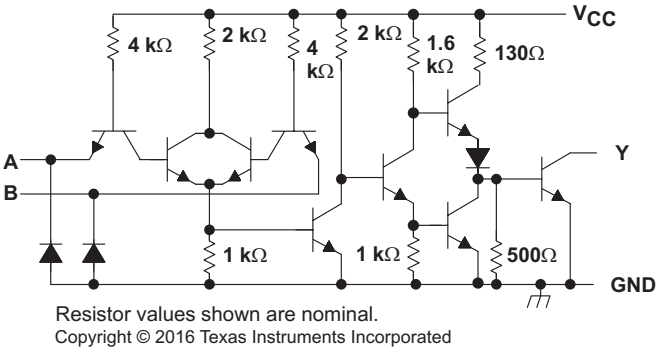


Figure 17. SNx5454B Schematic (Each Driver)

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typically the SN75451B device drives a high-voltage or high-current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of the SN75451B device, driving an LED using one channel and a high voltage peripheral using the other. In this configuration, the LED will turn on whenever the high voltage peripheral is on.

10.2 Typical Application

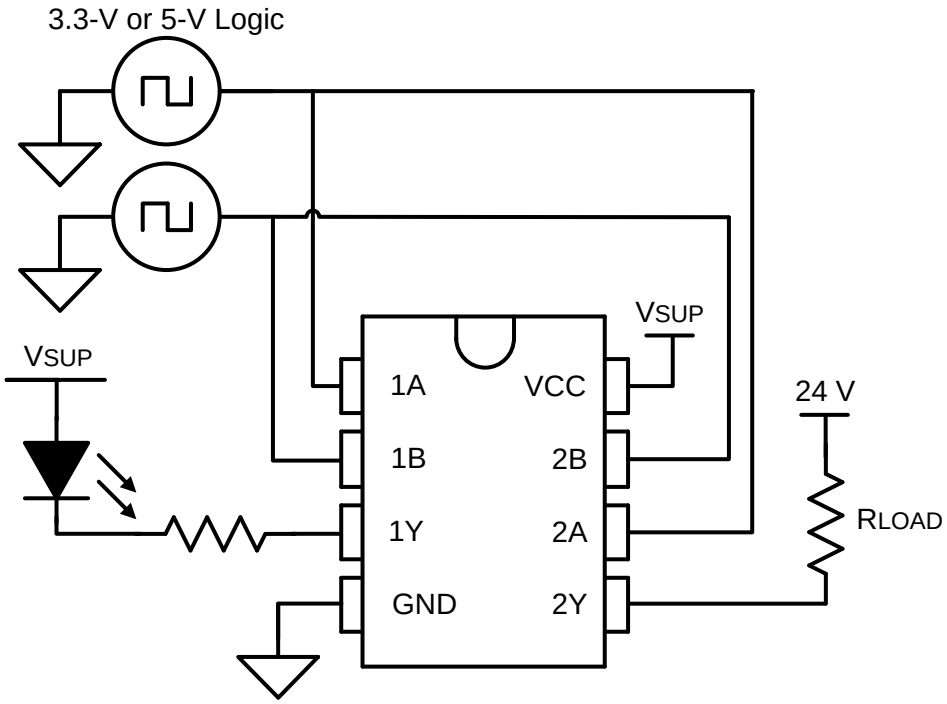


Figure 18. SN75451B Driving an LED and a High Voltage Peripheral

10.2.1 Design Requirements

Each of the inputs to the logic gate should never float. If one of the inputs is floating, then the logic gate could be in an unknown state. Be sure to connect ground or V_{CC} to any unused input channels.

10.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For specified high and low levels, see V_{IH} and V_{IL} in *Recommended Operating Conditions*.
   - The input voltage must not exceed the V_I specified in *Absolute Maximum Ratings*.
2. Recommended Output Conditions:
   - It is recommended that the load current not exceed 300 mA.
   - The load current must never exceed the I_{OK} noted in *Absolute Maximum Ratings*.

Typical Application (continued)

10.2.3 Application Curves

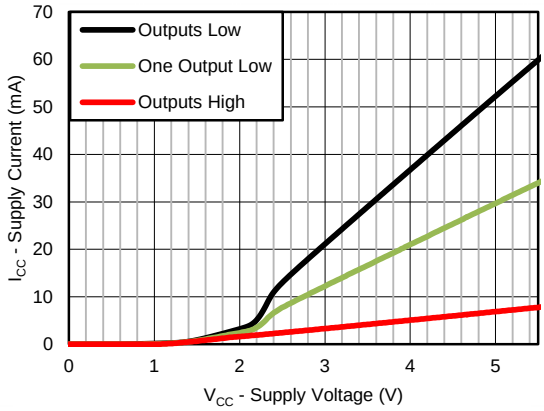


Figure 19. SN75451B Typical Supply Current vs Supply Voltage

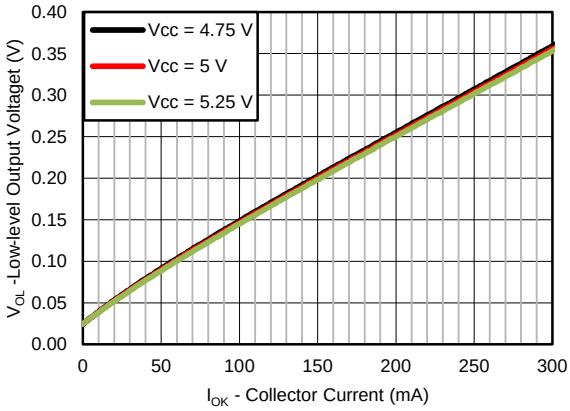


Figure 20. SN75451B Typical Low-Level Output Voltage vs Collector Current

11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in *Recommended Operating Conditions*. The V_{CC} pin should have a bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is suitable for this device.

12 Layout

12.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is used to drive the SNx545xB devices. Take care to separate the input channels to eliminate crosstalk. These traces are recommended for the output to be able to drive high currents. Be sure to connect ground or V_{CC} to any unused input channels, and use a bypass capacitor on the V_{CC} pin to prevent any power glitches.

12.2 Layout Example

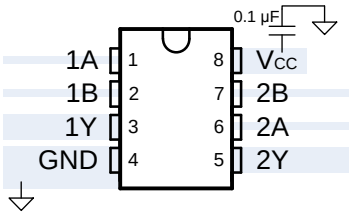


Figure 21. SN75451BD Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN55451B	Click here	Click here	Click here	Click here	Click here
SN55452B	Click here	Click here	Click here	Click here	Click here
SN55453B	Click here	Click here	Click here	Click here	Click here
SN55454B	Click here	Click here	Click here	Click here	Click here
SN75451B	Click here	Click here	Click here	Click here	Click here
SN75452B	Click here	Click here	Click here	Click here	Click here
SN75453B	Click here	Click here	Click here	Click here	Click here
SN75454B	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9563301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9563301Q2A SNJ55453BFK	Samples
5962-9563301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9563301QPA SNJ55453B	Samples
77049012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049012A SNJ55452BFK	Samples
7704901PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704901PA SNJ55452B	Samples
77049022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049022A SNJ55451BFK	Samples
7704902PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704902PA SNJ55451B	Samples
JM38510/12902BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12902BPA	Samples
JM38510/12903BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12903BPA	Samples
JM38510/12905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12905BPA	Samples
M38510/12902BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12902BPA	Samples
M38510/12903BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12903BPA	Samples
M38510/12905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/12905BPA	Samples
SN55451BJG	ACTIVE	CDIP	JG	8	50	TBD	A42	N / A for Pkg Type	-55 to 125	SN55451BJG	Samples
SN55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55452BJG	Samples
SN55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55453BJG	Samples
SN55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55454BJG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75451BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75451BP	Samples
SN75451BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75451BP	Samples
SN75451BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A451B	Samples
SN75452BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75452BP	Samples
SN75452BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75452BP	Samples
SN75452BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples
SN75452BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples
SN75452BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75453BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75453BP	Samples
SN75453BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75453BP	Samples
SN75453BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A453B	Samples
SN75454BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B	Samples
SN75454BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B	Samples
SN75454BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75454BP	Samples
SN75454BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75454BP	Samples
SN75454BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A454B	Samples
SNJ55451BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049022A SNJ55 451BFK	Samples
SNJ55451BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704902PA SNJ55451B	Samples
SNJ55452BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049012A SNJ55 452BFK	Samples
SNJ55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704901PA SNJ55452B	Samples
SNJ55453BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9563301Q2A SNJ55	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										453BFK	
SNJ55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9563301QPA SNJ55453B	Samples
SNJ55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ55 454BJG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

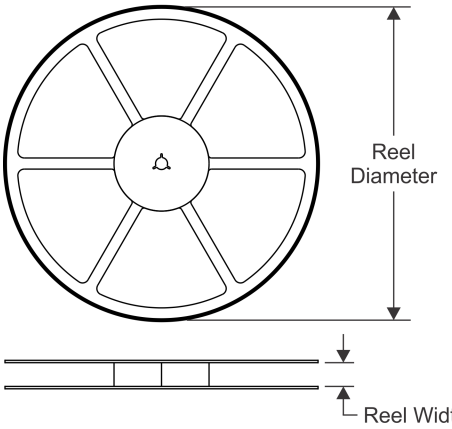
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

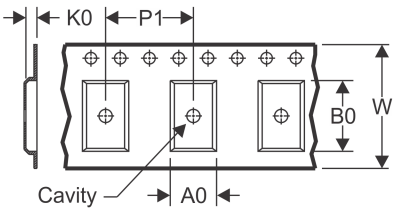
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

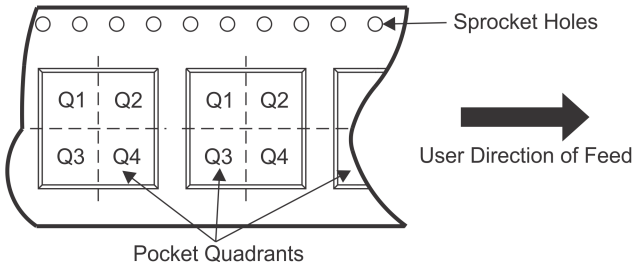


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

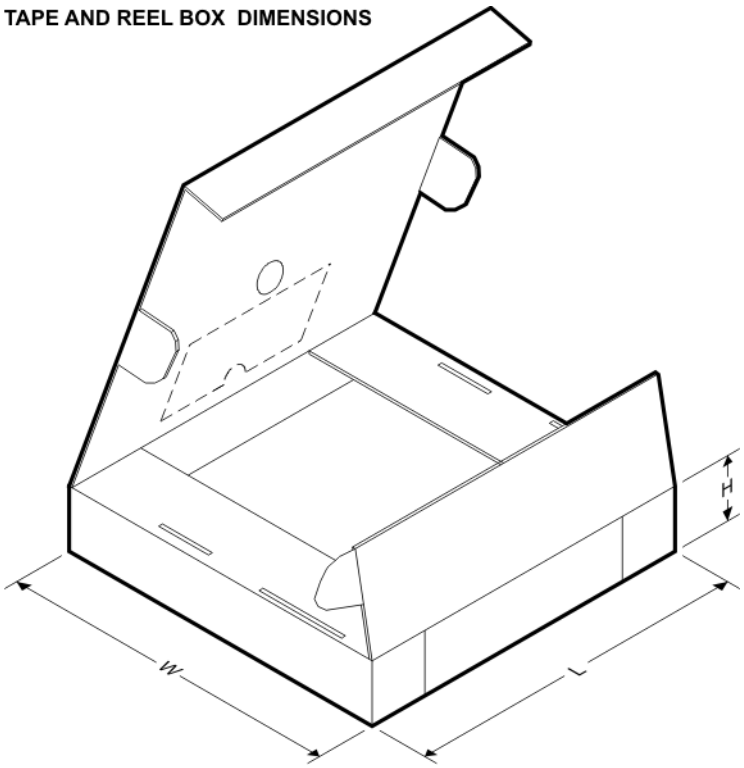
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75451BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75451BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75452BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75452BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75453BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75453BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75454BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75454BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

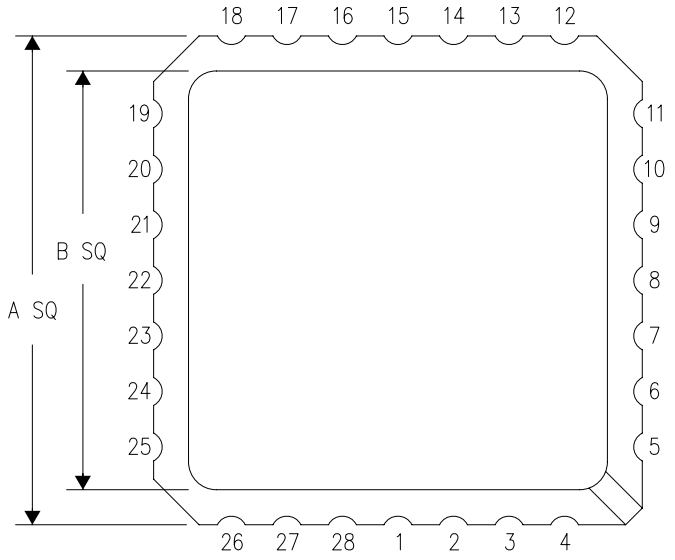


*All dimensions are nominal

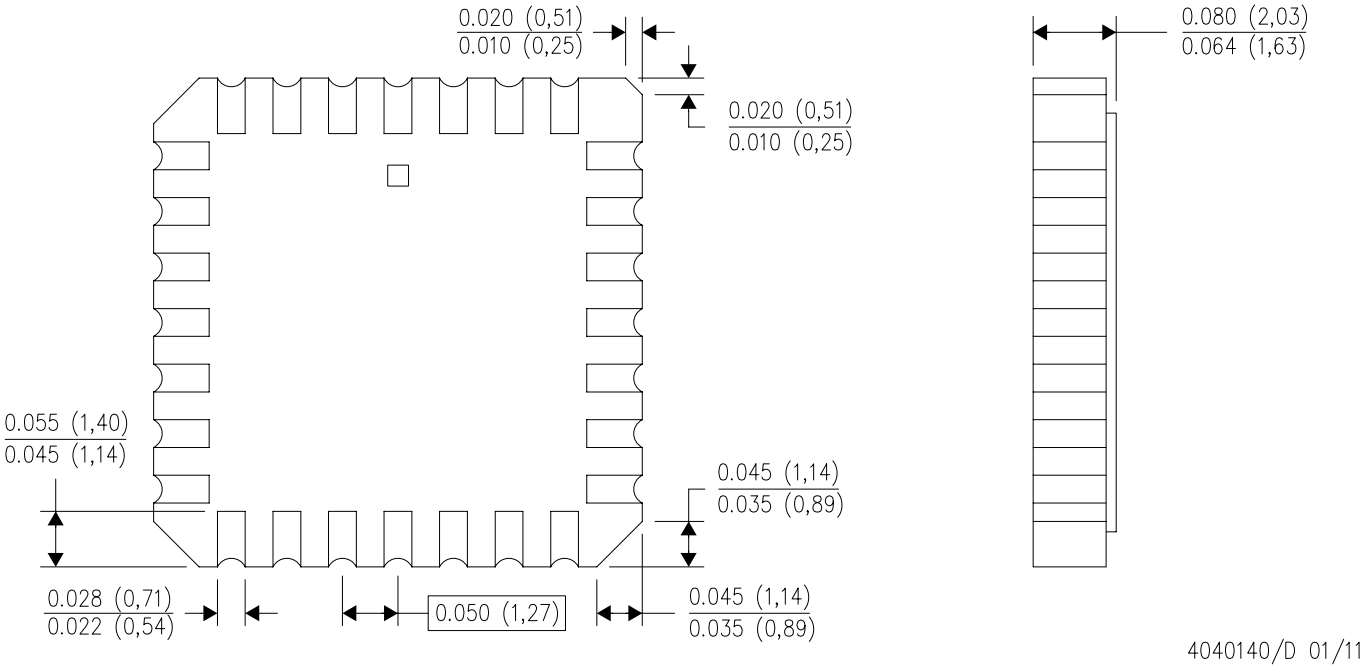
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75451BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75451BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75452BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75452BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75453BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75453BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75454BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75454BPSR	SO	PS	8	2000	367.0	367.0	38.0

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



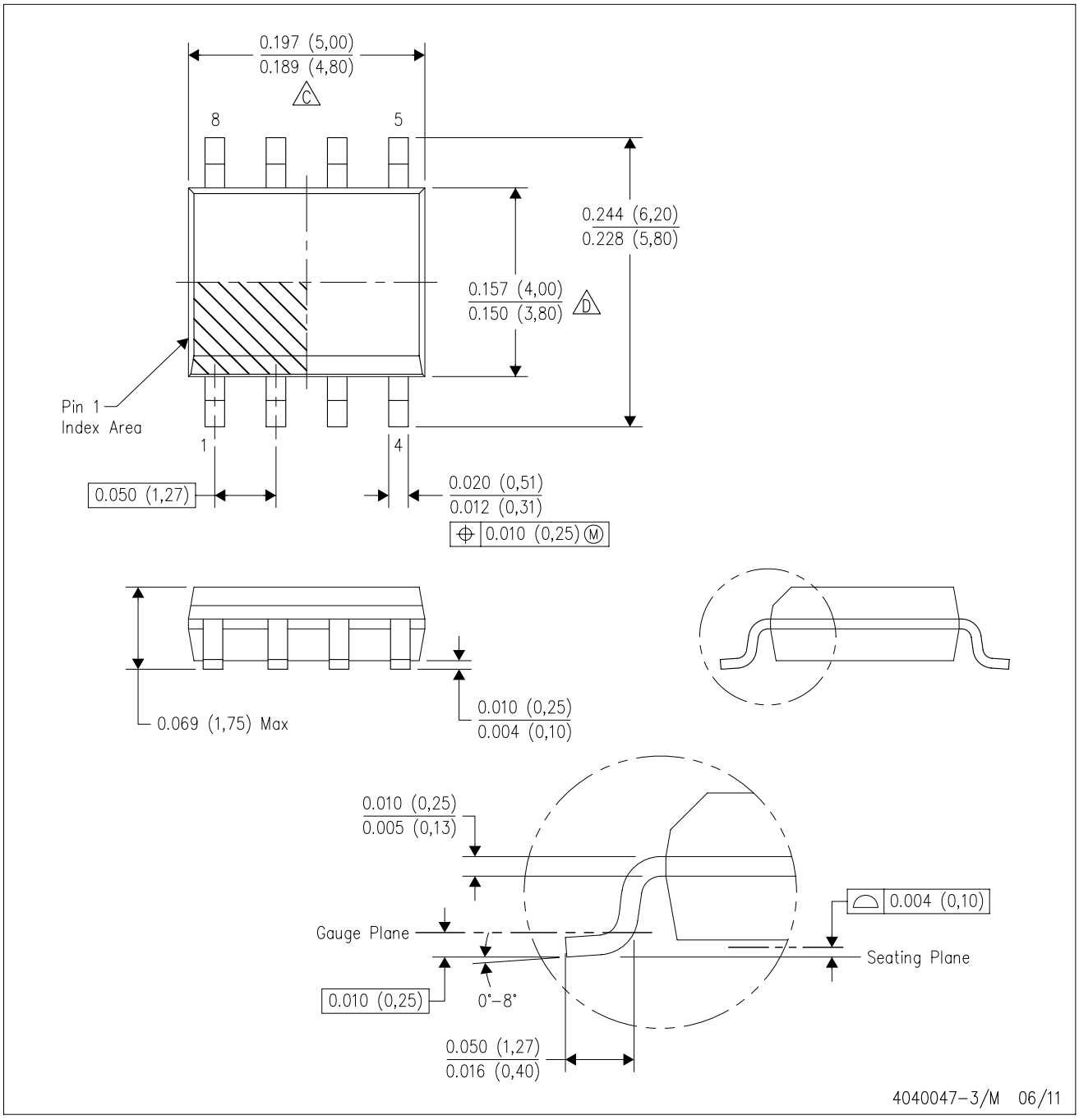
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

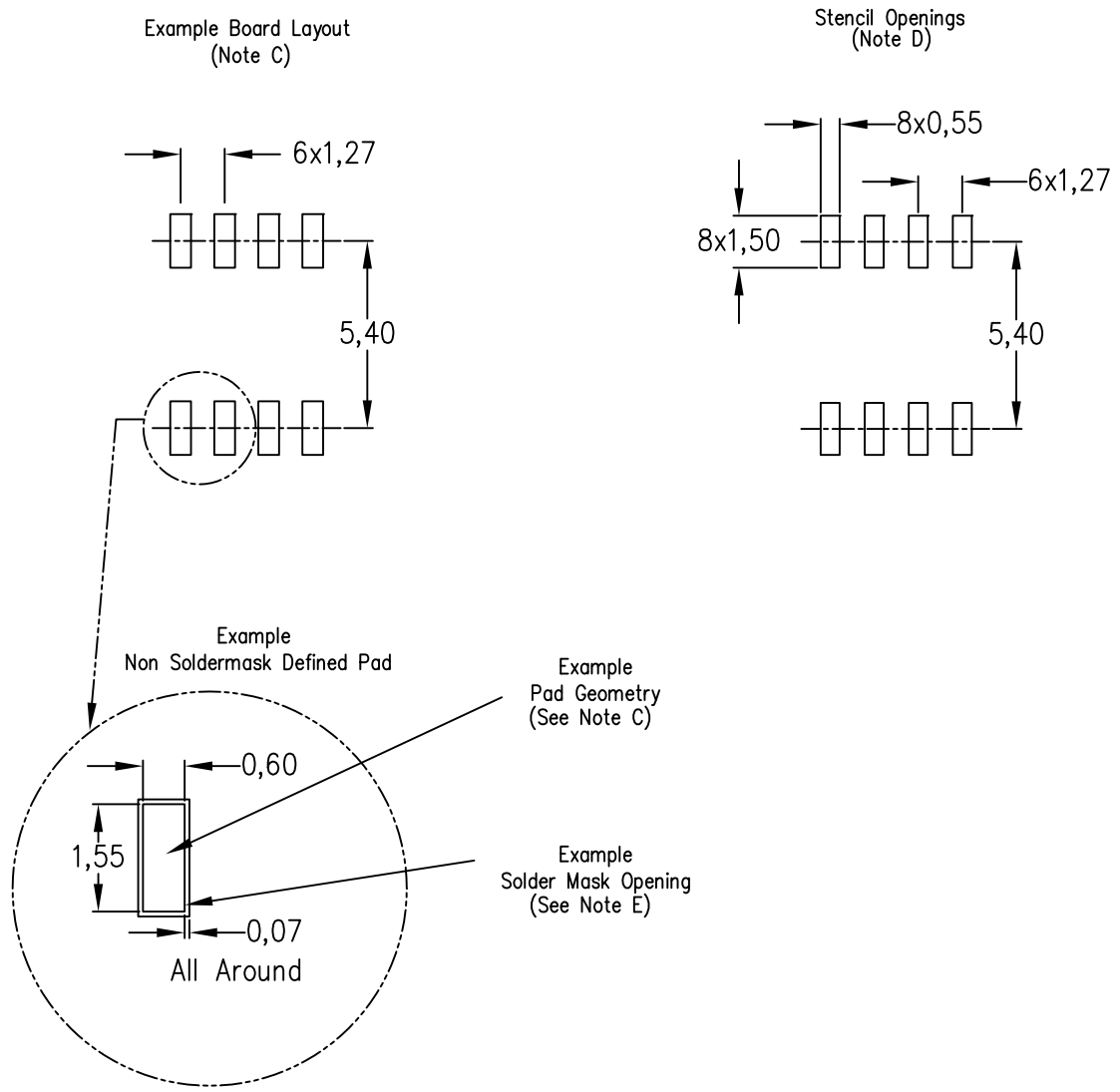
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

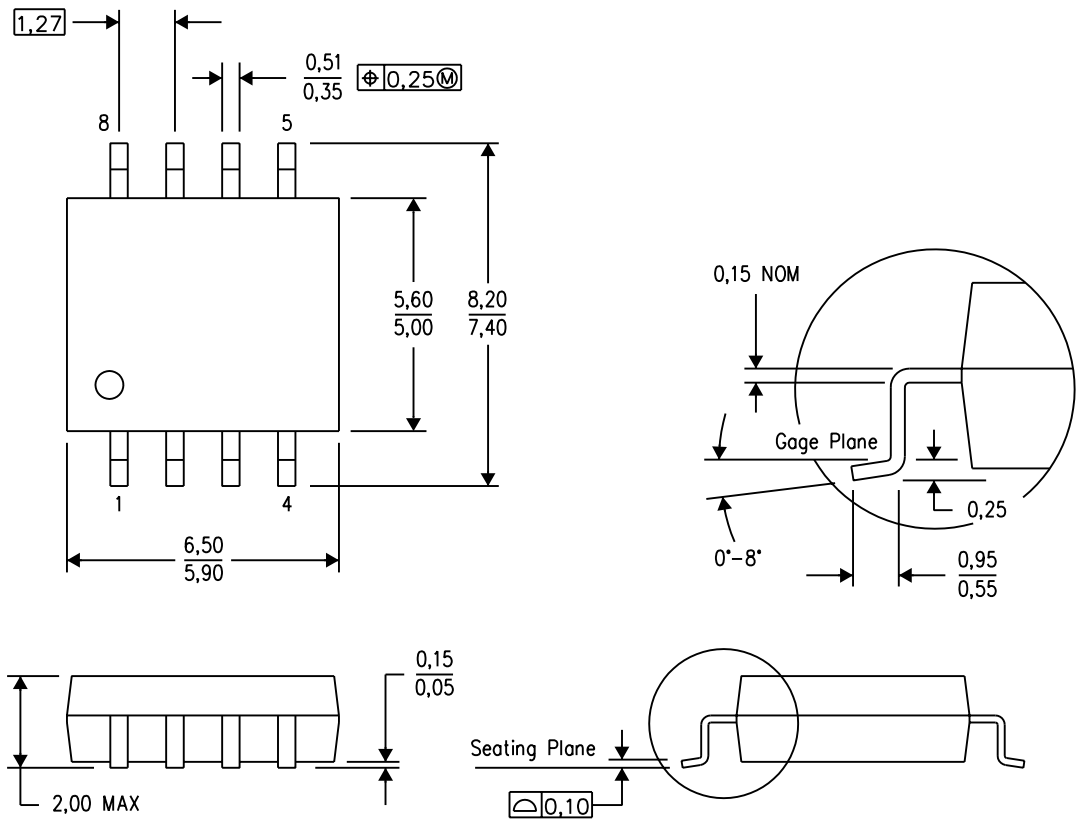
D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

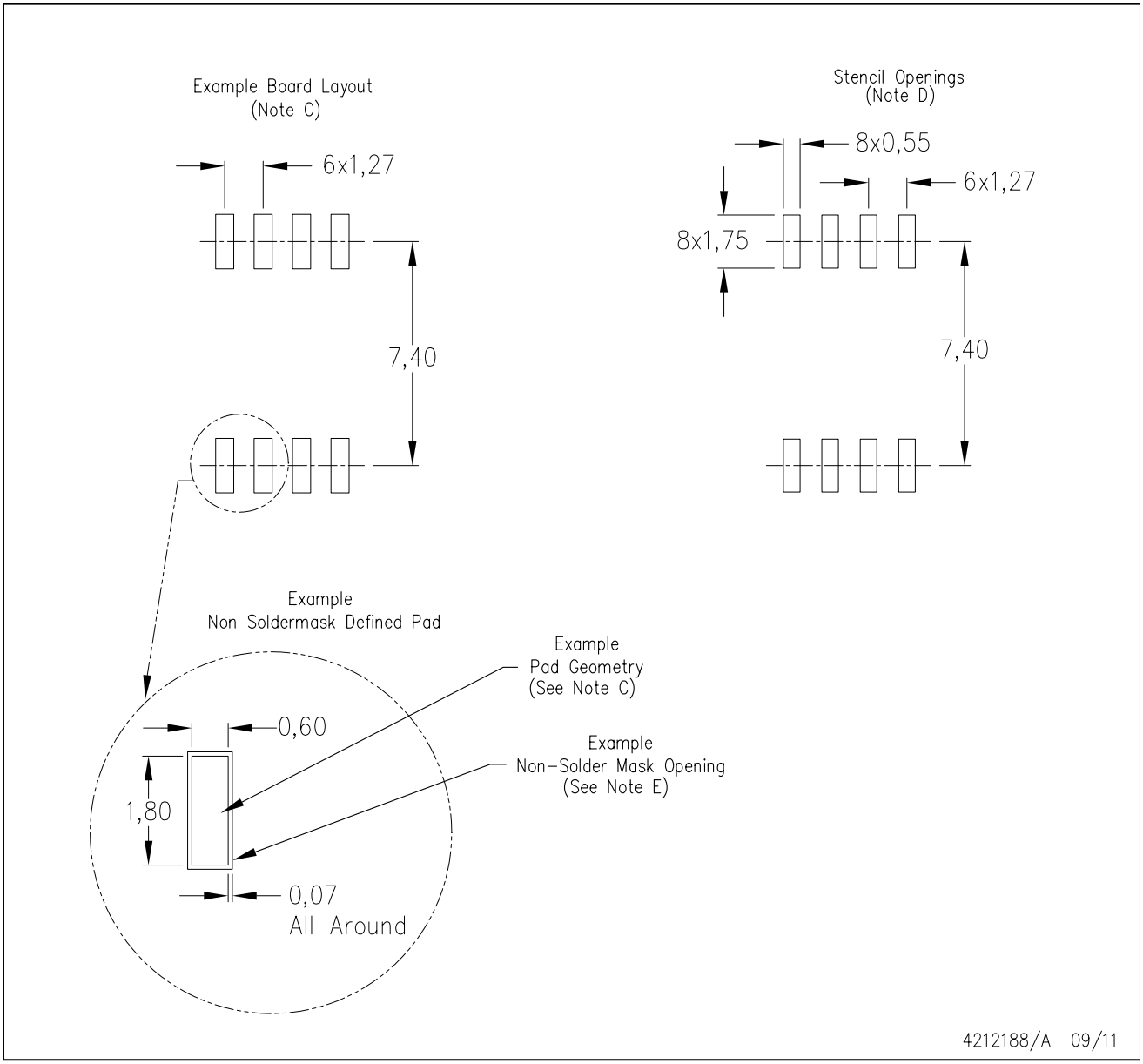
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

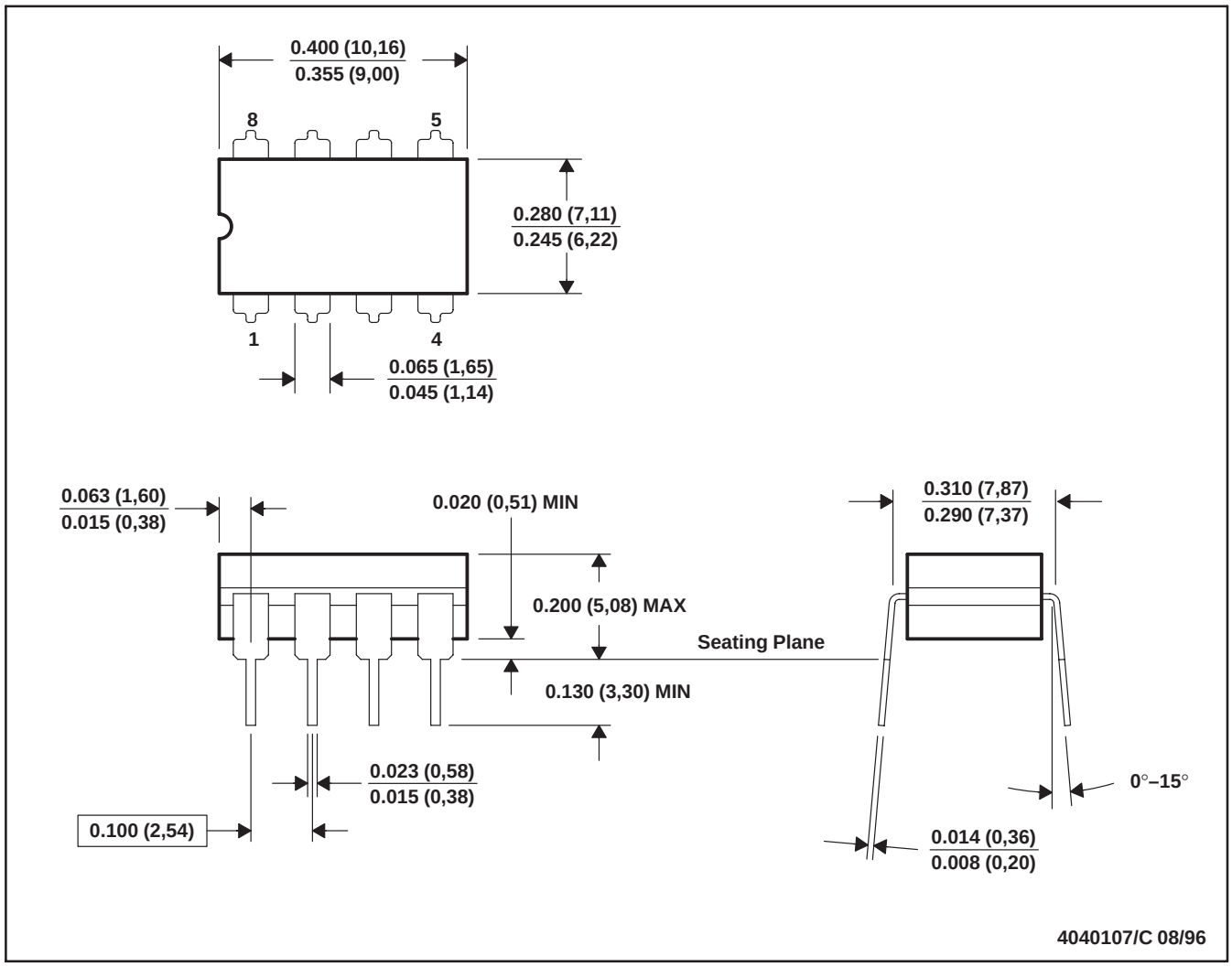
PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

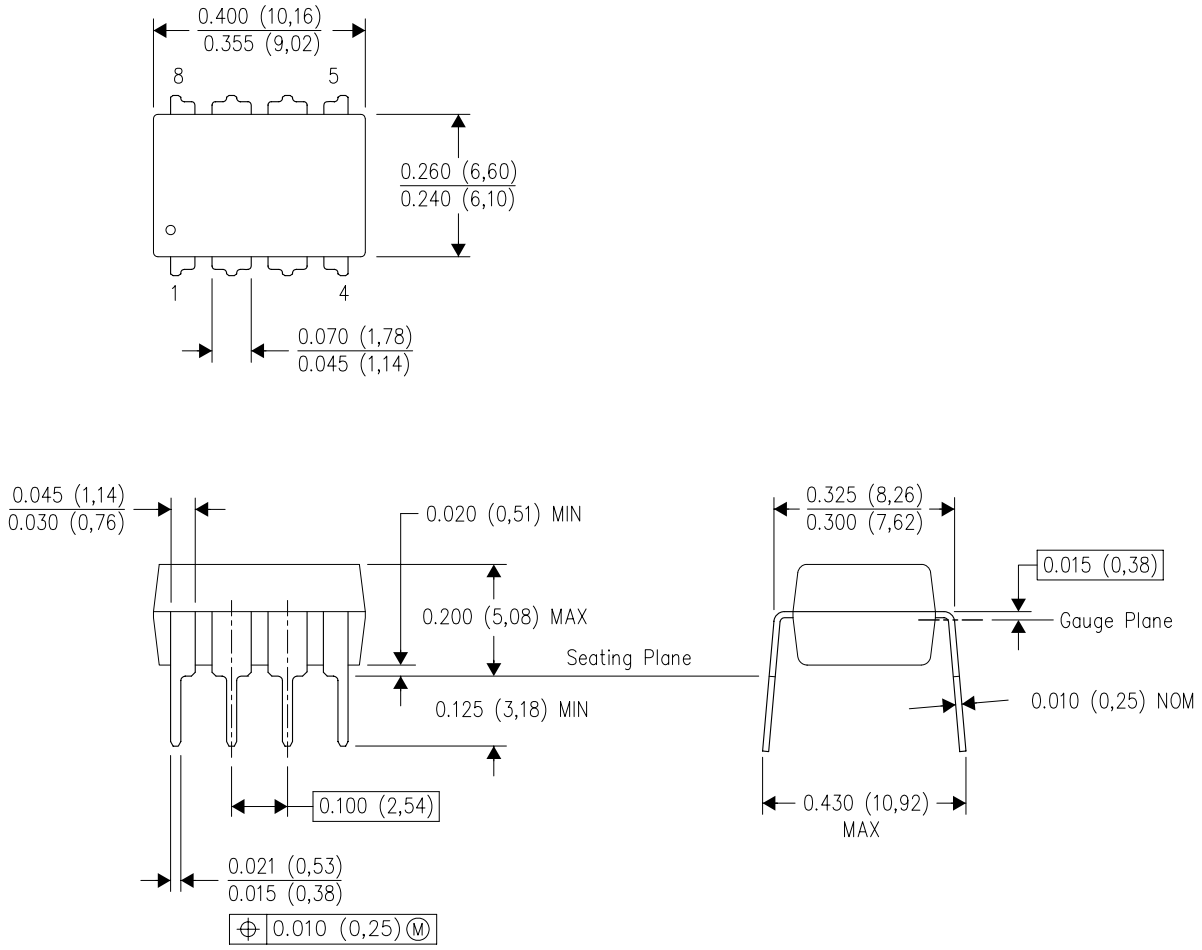
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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