# PCF8566

## Universal LCD driver for low multiplex rates

Rev. 07 — 25 February 2009 Product data sheet

## 1. General description

The PCF8566 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD) with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 24 segments and can easily be cascaded for larger LCD applications. The PCF8566 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional $I^2C$-bus. Communication overheads are minimized by a display RAM with auto-incremented addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

## 2. Features

- Single-chip LCD controller/driver
- 24 segment drives:
  - Up to twelve 7-segment numeric characters including decimal pointer
  - Up to six 14-segment alphanumeric characters
  - Any graphics of up to 96 elements
- Versatile blinking modes
- No external components required (even in multiple device applications)
- Selectable backplane drive configuration: static or 2, 3, 4 backplane multiplexing
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Internal LCD bias generation with voltage-follower buffers
- 24 $\times$ 4-bit RAM for display data storage
- Auto-incremented display data loading across device subaddress boundaries
- Display memory bank switching in static and duplex drive modes
- LCD and logic supplies may be separated
- 2.5 V to 6 V power supply range
- Low power consumption
- Power-saving mode for extremely low power consumption in battery-operated and telephone applications
- $I^2C$-bus interface
- TTL and CMOS compatible
- Compatible with any 4, 8 or 16-bit microprocessor or microcontroller
- May be cascaded for large LCD applications (up to 1536 segments possible)
- Cascadable with 40-segment LCD driver PCF8576C
- Optimized pinning for plane wiring in both and multiple PCF8566 applications
- Space-saving 40-lead plastic very small outline package (VSO40; SOT158-1)
- Manufactured in silicon gate CMOS process

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PCF8566P | DIP40 | plastic dual in-line package; 40 leads (600 mil) | SOT129-1 |
| PCF8566T | VSO40 | plastic very small outline package; 40 leads | SOT158-1 |
| PCF8566TS[1] | VSO40 | plastic very small outline package; 40 leads | SOT158-1 |
| PCF8566U[2] | PCF8566U | wire bond die; 40 bonding pads; $2.5 \times 2.91 \times 0.381$ mm | PCF8566U |

[1] Dark-green version.

[2] Chip in tray for chip on board.

## 4. Marking

**Table 2. Marking codes**

| Type number | Marking code |
|---|---|
| PCF8566P | PCF8566P |
| PCF8566T | PCF8566T |
| PCF8566TS | PCF8566TS |
| PCF8566U | PC8566-1 |

## 5. Block diagram

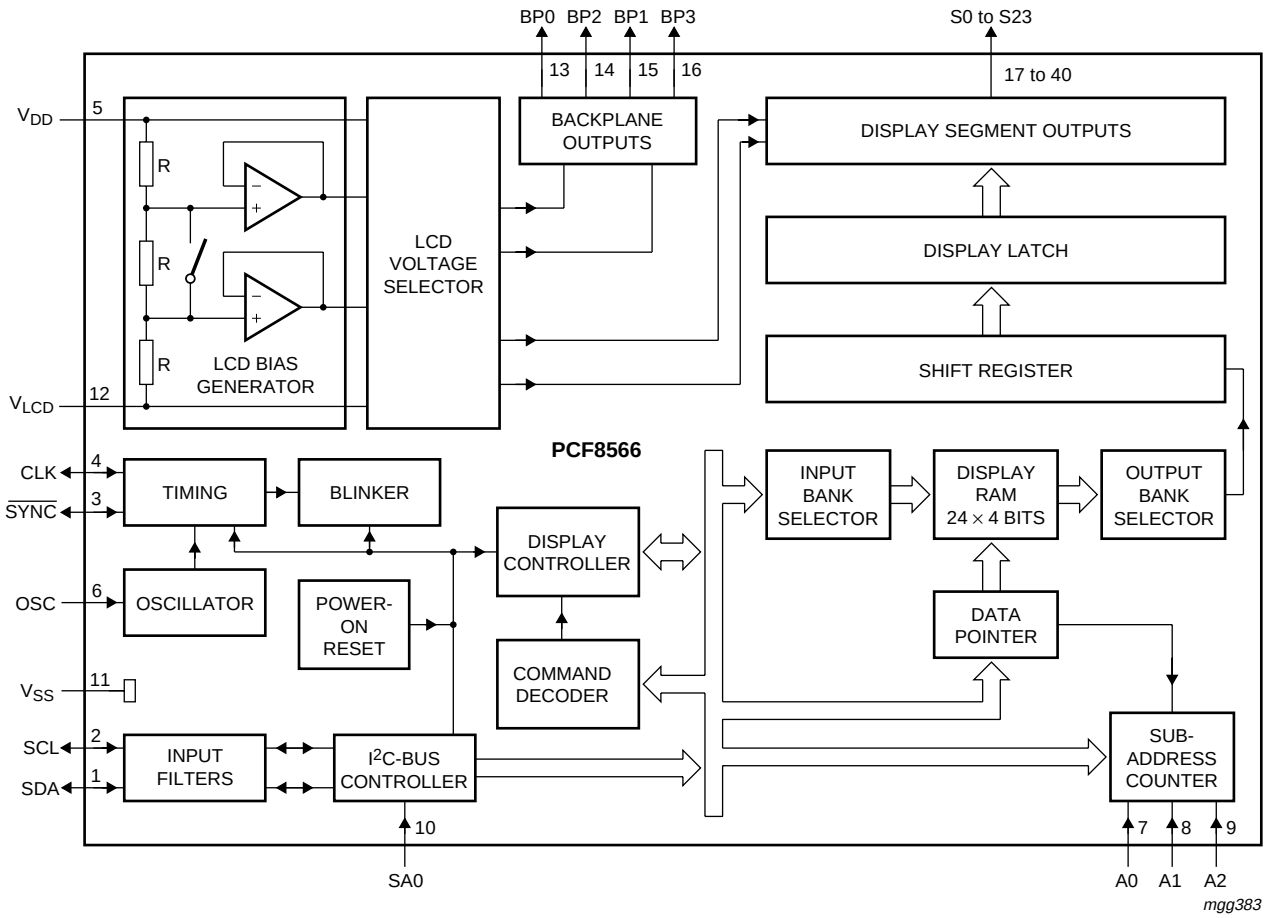



**Fig 1. Block diagram of PCF8566**

# 6. Pinning information

## 6.1 Pinning

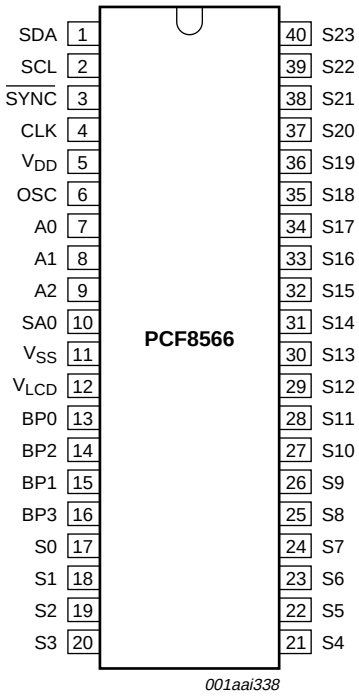



**Fig 2. Pin configuration for PCF8566**

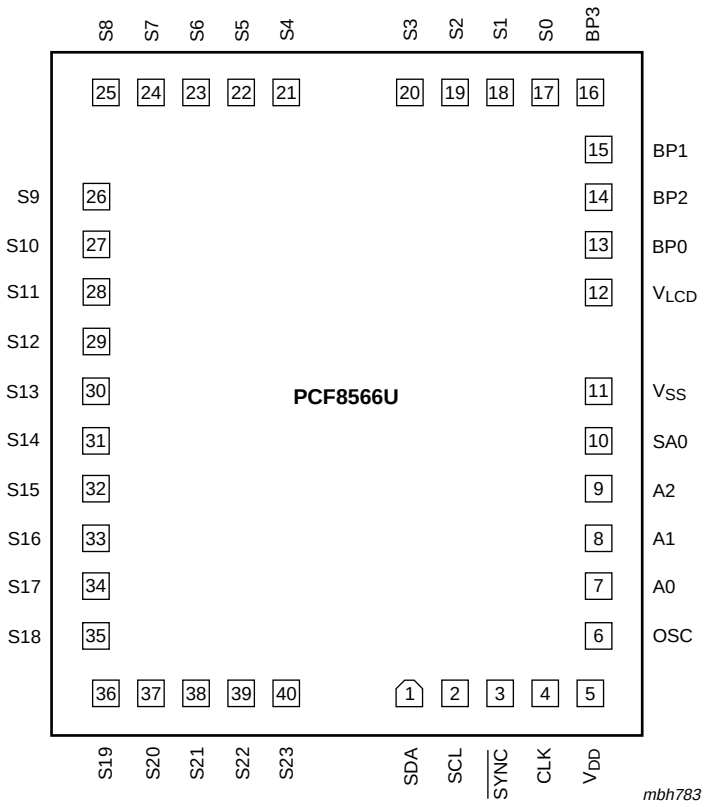



**Fig 3. Pin configuration for PCF8566U**

## 6.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| SDA | 1 | $I^2C$-bus data input and output |
| SCL | 2 | $I^2C$-bus clock input and output |
| $\overline{SYNC}$ | 3 | cascade synchronization input and output |
| CLK | 4 | external clock input and output |
| $V_{DD}$ | 5 | positive supply voltage[1] |
| OSC | 6 | oscillator select |
| A0 | 7 | $I^2C$-bus subaddress inputs |
| A1 | 8 | |
| A2 | 9 | |
| SA0 | 10 | $I^2C$-bus slave address bit 0 input |
| $V_{SS}$ | 11 | logic ground |
| $V_{LCD}$ | 12 | LCD supply voltage |

**Table 3. Pin description** *...continued*

| Symbol | Pin | Description |
|---|---|---|
| BP0 | 13 | LCD backplane outputs |
| BP2 | 14 | |
| BP1 | 15 | |
| BP3 | 16 | |
| S0 to S23 | 17 to 40 | LCD segment outputs |

[1] The substrate (rear side of the die) is wired to $V_{DD}$ but should not be electrically connected.

# 7. Functional description

The PCF8566 is a versatile peripheral device designed to interface any microprocessor or microcontroller to a wide variety of LCDs. It can directly drive any static or multiplexed LCD containing up to 4 backplanes and up to 24 segments.

The display configurations possible with the PCF8566 depend on the number of active backplane outputs required. Display configuration selection is shown in Table 4. All of the display configurations given in Table 4 can be implemented in the typical system shown in Figure 4.

The host microprocessor or microcontroller maintains the 2-line $I^2C$-bus communication channel with the PCF8566.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to $V_{SS}$. The only other connections required to complete the system are the power supplies (pins $V_{DD}$, $V_{SS}$ and $V_{LCD}$) and the LCD panel selected for the application.

**Table 4. Display configurations**

| Backplanes | Elements | 7-segment numeric | | 14-segment numeric | | Dot matrix |
|---|---|---|---|---|---|---|
| | | Digits | Indicator symbols | Characters | Indicator symbols | |
| 4 | 96 | 12 | 12 | 6 | 12 | 96 (4 × 24) |
| 3 | 72 | 9 | 9 | 4 | 16 | 72 (3 × 24) |
| 2 | 48 | 6 | 6 | 3 | 6 | 48 (2 × 24) |
| 1 | 24 | 3 | 3 | 1 | 10 | 24 |

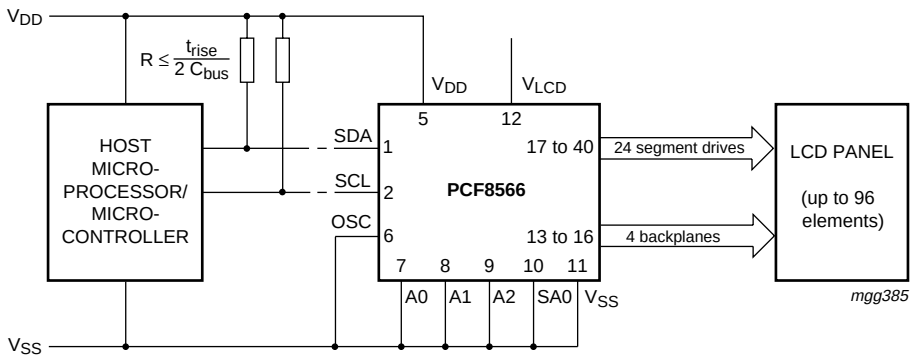



**Fig 4. Typical system configuration**

## 7.1 Power-on reset

At power-on the PCF8566 resets to the following starting conditions:

- All backplane outputs are set to $V_{DD}$
- All segment outputs are set to $V_{DD}$
- Drive mode 1:4 multiplex with $\frac{1}{3}$ bias is selected
- Blinking is switched off
- Input and output bank selectors are reset (as defined in Table 8)
- The $I^2C$-bus interface is initialized
- The data pointer and the subaddress counter are cleared

Do not transfer data on the $I^2C$-bus after a power-on for at least 1 ms to allow the reset action to complete.

## 7.2 LCD bias generator

The full-scale LCD voltage ($V_{oper}$) is obtained from $V_{DD} - V_{LCD}$. The LCD voltage may be temperature compensated externally through the $V_{LCD}$ supply to pin 12.

Fractional LCD biasing voltages are obtained from an internal voltage divider comprising three series resistors connected between $V_{DD}$ and $V_{LCD}$. The center resistor can be switched out of the circuit to provide a $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration.

## 7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by mode-set commands from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of $V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 5.

**Table 5. Preferred LCD drive modes: summary of characteristics**

| LCD drive mode | Number of: | | LCD bias configuration | $\frac{V_{off(RMS)}}{V_{LCD}}$ | $\frac{V_{on(RMS)}}{V_{LCD}}$ | $D = \frac{V_{on(RMS)}}{V_{off(RMS)}}$ |
|---|---|---|---|---|---|---|
| | Backplanes | Bias levels | | | | |
| static | 1 | 2 | static | 0 | 1 | ∞ |
| 1:2 multiplex | 2 | 3 | ½ | 0.354 | 0.791 | 2.236 |
| 1:2 multiplex | 2 | 4 | ⅓ | 0.333 | 0.745 | 2.236 |
| 1:3 multiplex | 3 | 4 | ⅓ | 0.333 | 0.638 | 1.915 |
| 1:4 multiplex | 4 | 4 | ⅓ | 0.333 | 0.577 | 1.732 |

A practical value for $V_{LCD}$ is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th}$), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with ½ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for ½ bias

a = 2 for ⅓ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with the equation

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{\frac{1}{n} + \left[(n-1)\times\left(\frac{1}{1+a}\right)\right]^2}{n}} \quad (1)$$

where $V_{LCD}$ is the resultant voltage at the LCD segment and where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with the equation:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - (2a+n)}{n\times(1+a)^2}} \quad (2)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from the equation:

$$\frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \quad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of

- 1:3 multiplex with ½ bias is $\sqrt{3} = 1.732$

- 1:4 multiplex with ½ bias is $\frac{\sqrt{21}}{3} = 1.528$

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage $V_{LCD}$ as follows:

- 1:3 multiplex (½ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$
- 1:4 multiplex (½ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

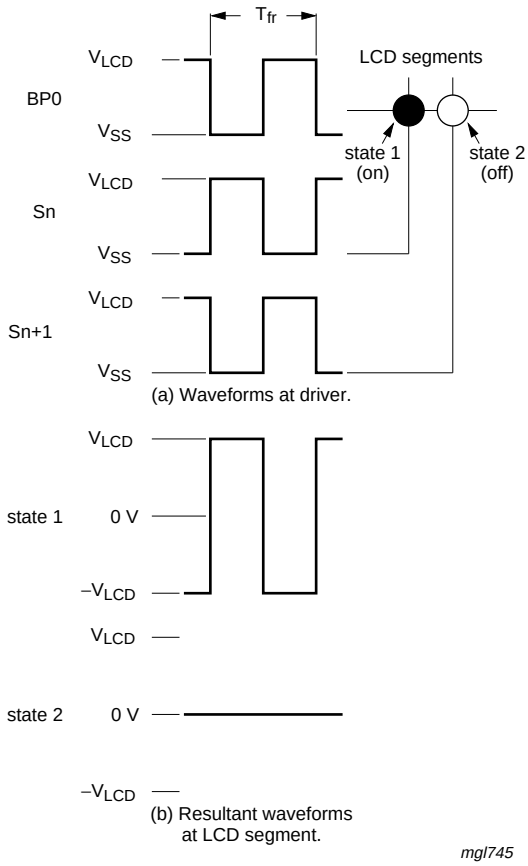
These compare with $V_{LCD} = 3 V_{off(RMS)}$ when ⅓ bias is used.

It should be noted that $V_{LCD}$ is sometimes referred as the LCD operating voltage.

## 7.4 LCD drive mode waveforms

### 7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 5.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = V_{LCD}$.

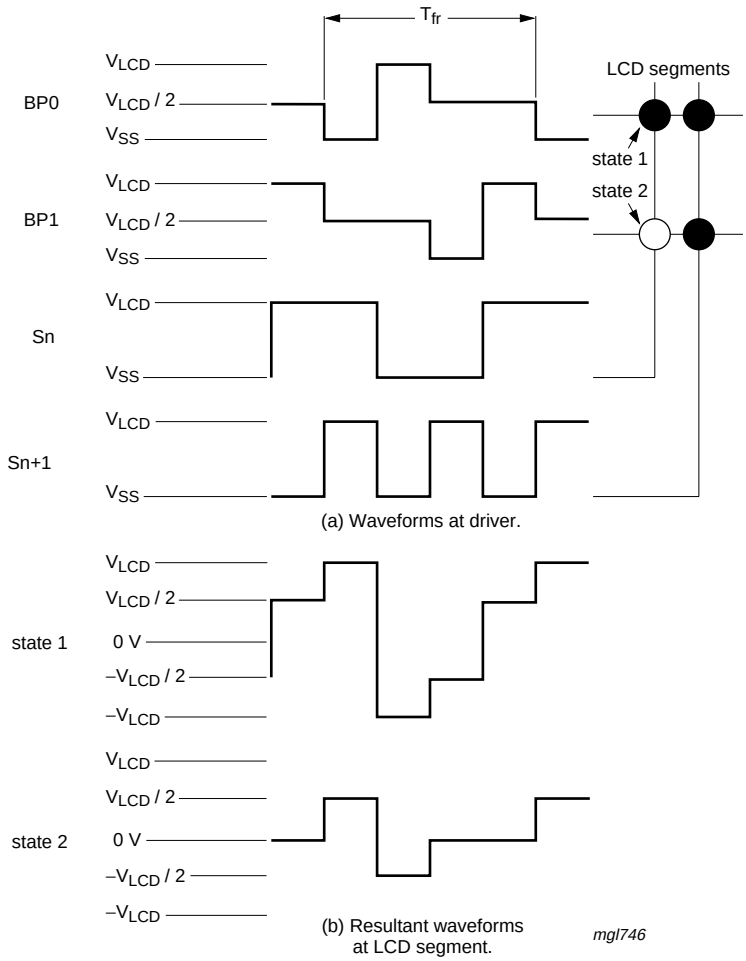
$V_{state2}(t) = V_{Sn+1}(t) - V_{BP0}(t)$.

$V_{off(RMS)} = 0$ V.

**Fig 5. Static drive mode waveforms**

### 7.4.2 1:2 Multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8566 allows the use of ½ bias or ⅓ bias (see Figure 6 and Figure 7).



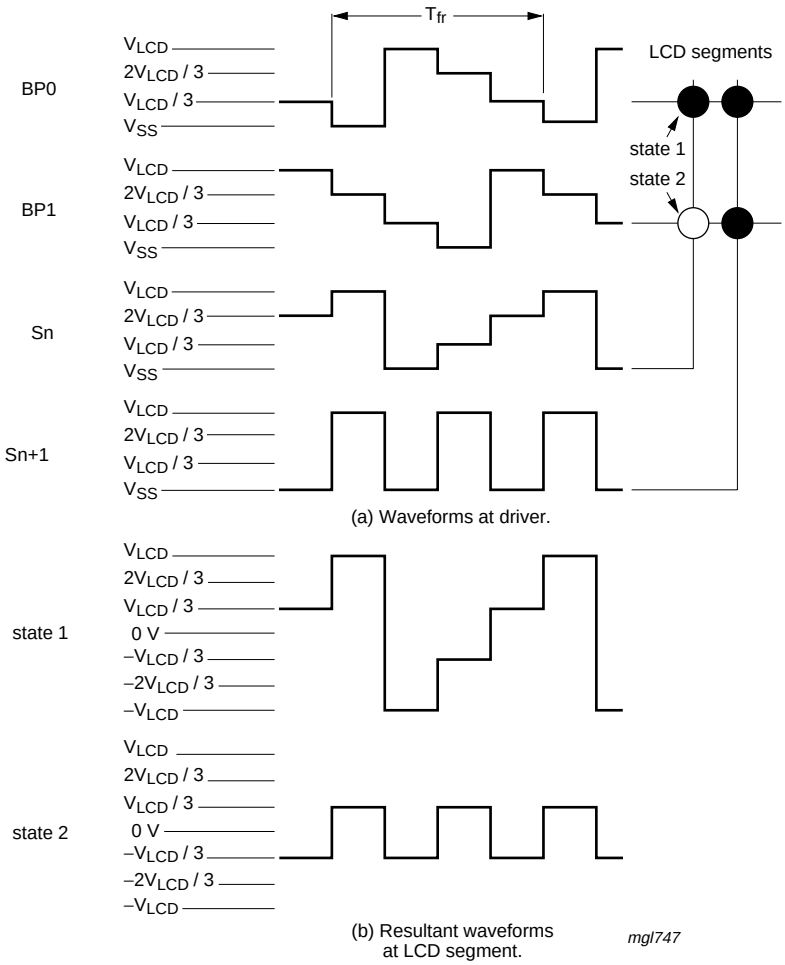

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354V_{LCD}$

**Fig 6. Waveforms for the 1:2 multiplex drive mode with ½ bias**




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.745V_{LCD}$

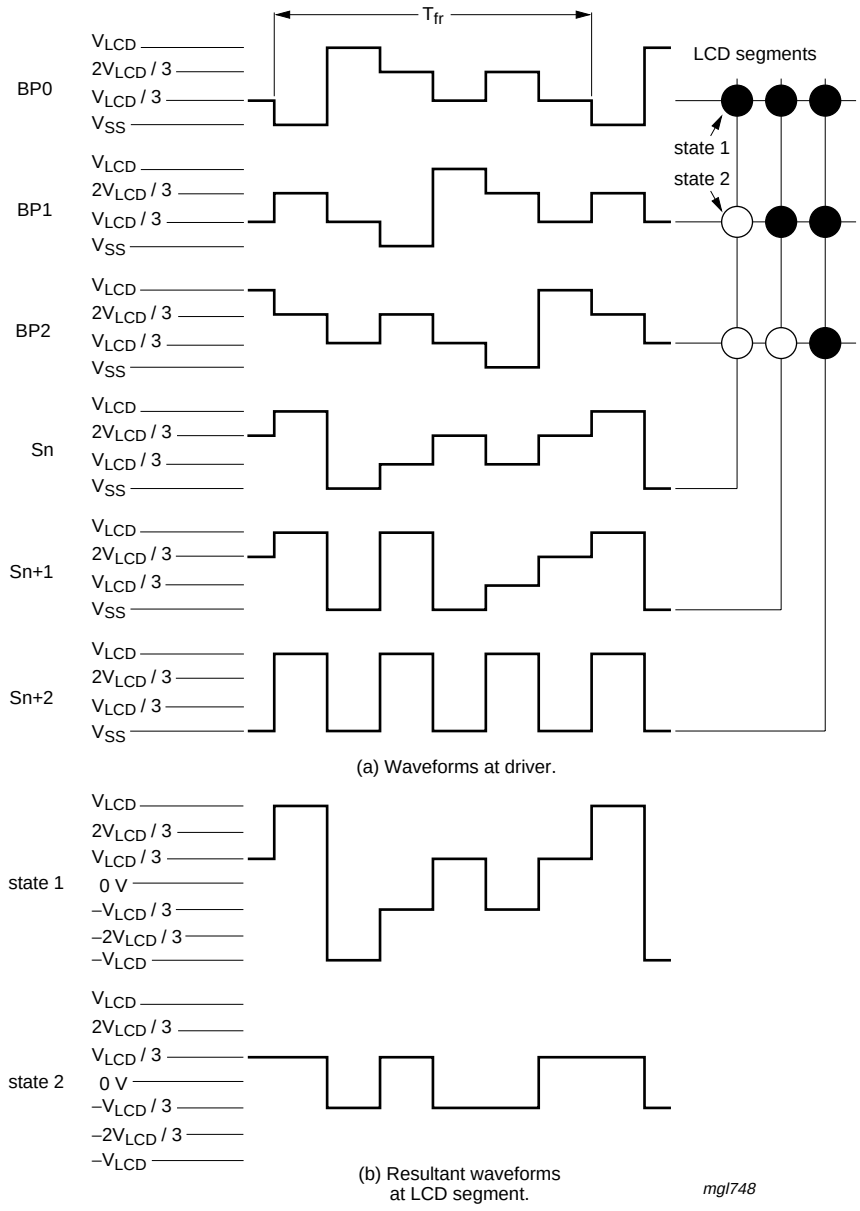
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$

$V_{off(RMS)} = 0.333V_{LCD}$.

**Fig 7. Waveforms for the 1:2 multiplex drive mode with $^1/_3$ bias**

### 7.4.3 1:3 Multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 8.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

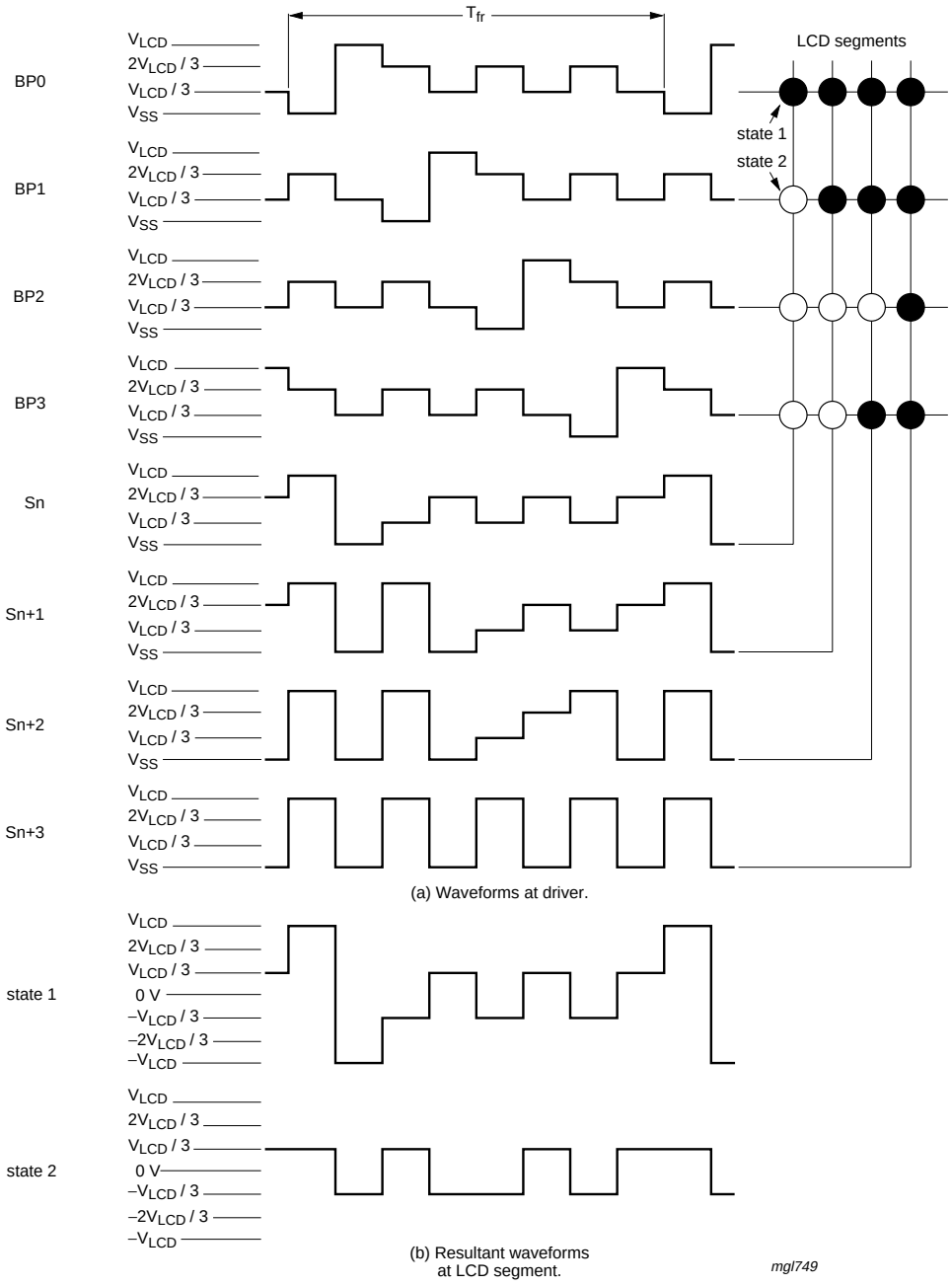
$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

**Fig 8. Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias**

### 7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies, as shown in Figure 9.




$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

**Fig 9. Waveforms for the 1:4 multiplex mode with ⅓ bias**

## 7.5 Oscillator

The internal logic and the LCD drive signals of the PCF8566 are timed by the frequency $f_{clk}$, which equals either the built-in oscillator frequency $f_{osc}$ or the external clock frequency $f_{clk(ext)}$.

The clock frequency ($f_{clk}$) determines the LCD frame frequency ($f_{fr}$) and the maximum rate for data reception from the $I^2C$-bus. To allow $I^2C$-bus transmissions at their maximum data rate of 100 kHz, $f_{clk}$ should be chosen to be above 125 kHz.

### 7.5.1 Internal clock

The internal oscillator is enabled by connecting pin OSC to pin $V_{SS}$. In this case, the output from pin CLK is the clock signal for any cascaded PCF8566s or PCF8576s in the system.

### 7.5.2 External clock

Connecting pin OSC to $V_{DD}$ enables an external clock source. Pin CLK then becomes the external clock input.

**Remark:** A clock signal must always be supplied to the device. Removing the clock, freezes the LCD in a DC state.

## 7.6 Timing

The timing of the PCF8566 sequences the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between the PCF8566s in the system. The timing also generates the LCD frame frequency which is derived as an integer division of the clock frequency (see Table 6). The frame frequency is set by the mode set commands when an internal clock is used or by the frequency applied to the pin CLK when an external clock is used.

**Table 6. LCD frame frequencies [1]**

| PCF8566 mode | Frame frequency | Nominal frame frequency (Hz) |
|---|---|---|
| normal mode | $f_{fr} = \frac{f_{clk}}{2880}$ | 69 [2] |
| power saving mode | $f_{fr} = \frac{f_{clk}}{480}$ | 65 [3] |

[1] The possible values for $f_{clk}$ see Table 20.

[2] For $f_{clk}$ = 200 kHz.

[3] For $f_{clk}$ = 31 kHz.

The ratio between the clock frequency and the LCD frame frequency depends on the mode in which the device is operating. In the power-saving mode the reduction ratio is six times smaller; this allows the clock frequency to be reduced by a factor of six. The reduced clock frequency results in a significant reduction in power dissipation.

The lower clock frequency has the disadvantage of increasing the response time when large amounts of display data are transmitted on the $I^2C$-bus. When a device is unable to process a display data byte before the next one arrives, it holds the SCL line LOW until the first display data byte is stored. This slows down the transmission rate of the $I^2C$-bus but no data loss occurs.

## 7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

## 7.8 Shift register

The shift register transfers display information from the display RAM to the display register while previous data is displayed.

## 7.9 Segment outputs

The LCD drive section includes 24 segment outputs S0 to S23 which must be connected directly to the LCD. The segment output signals are generated based on the multiplexed backplane signals and with data resident in the display register. When less than 24 segment outputs are required, the unused segment outputs should be left open-circuit.

## 7.10 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated based on the selected LCD drive mode.

- In 1:4 multiplex drive mode: BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left as an open-circuit.

- In 1:3 multiplex drive mode: BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode: BP0 and BP2, BP1 and BP3 respectively carry the same signals and can also be paired to increase the drive capabilities.
- In static drive mode: the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

## 7.11 Display RAM

The display RAM is a static 24 $\times$ 4-bit RAM which stores LCD data. Logic 1 in the RAM bit map indicates the on-state of the corresponding LCD segment; similarly, logic 0 indicates the off-state. There is a direct relationship between the RAM addresses and the segment outputs, and between the individual bits of a RAM word and the backplane outputs. The first RAM row corresponds to the 24 segments operated with respect to backplane BP0 (see Figure 10). In multiplexed LCD applications, the segment data of rows 1 to 4 of the display RAM are time-multiplexed with BP0, BP1, BP2 and BP3 respectively.

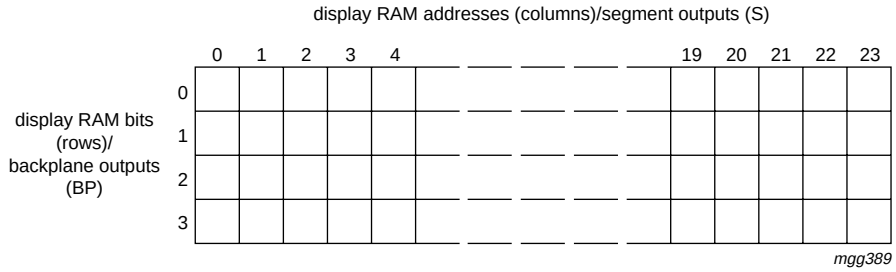



**Fig 10. Display RAM bit map showing the direct relationship between display RAM addresses and segment outputs and between bits in a RAM word and backplane outputs**

When display data is transmitted to the PCF8566 the display bytes received are stored in the display RAM based on the selected LCD drive mode. An example of a 7-segment numeric display illustrating the storage order for all drive modes is shown in Figure 11. The RAM storage organization applies equally to other LCD types.

The following applies to Figure 11:

- Static drive mode: the eight transmitted data bits are placed in row 0 to eight successive display RAM addresses.
- 1:2 multiplex drive mode: the eight transmitted data bits are placed in row 0 and 1 to four successive display RAM addresses.
- 1:3 multiplex drive mode: the eight transmitted data bits are placed in row 0, 1 and 2 of three successive addresses, with bit 2 of the third address left unchanged. This last bit can, if necessary, be controlled by an additional transfer to this address but avoid overriding adjacent data because always full bytes are transmitted.
- 1:4 multiplex drive mode: the eight transmitted data bits are placed in row 0, 1, 2 and 3 to two successive display RAM addresses.

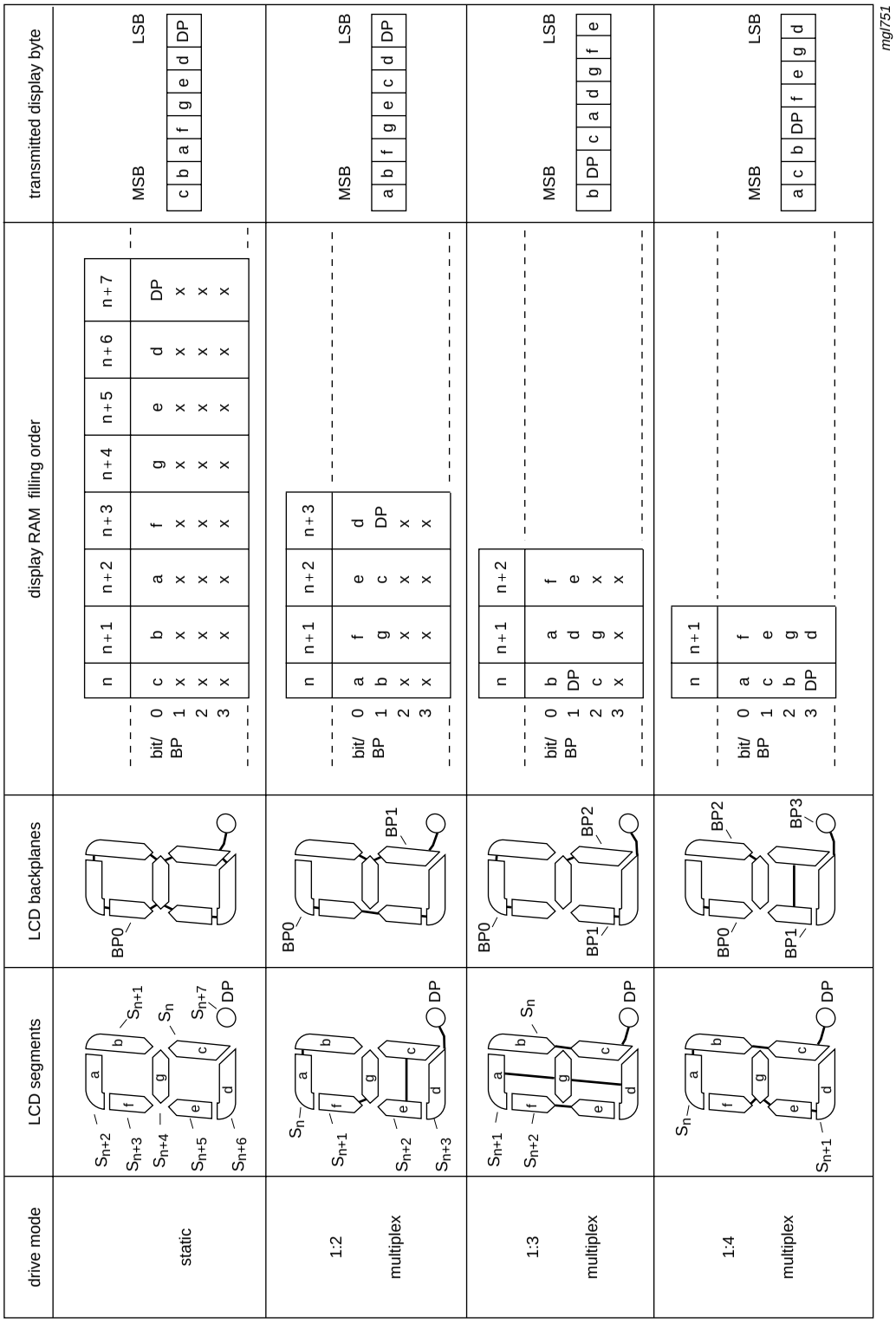
## 7.12 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load data pointer command (see Table 13). After this, the data byte is stored starting at the display RAM address indicated by the data pointer (see Figure 11). Once each byte is stored, the data pointer is automatically incremented based on the selected LCD configuration.

The contents of the data pointer are incremented as follows:

- In static drive mode by eight.
- In 1:2 multiplex drive mode by four.
- In 1:3 multiplex drive mode by three.
- In 1:4 multiplex drive mode by two.

If an $I^2C$-bus data access terminates early, the state of the data pointer is unknown. Consequently, the data pointer must be rewritten prior to further RAM accesses.




x = data bit unchanged

**Fig 11. Relationship between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus**

## 7.13 Sub-address counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed to take place only when the contents of the subaddress counter match with the hardware subaddress applied to A0, A1 and A2. The subaddress counter value is defined by the device select command (see Table 14 and Table 21). If the contents of the subaddress counter and the hardware subaddress do not match then data storage is blocked but the data pointer will be incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8566 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 14th display data byte transmitted in 1:3 multiplex mode).

## 7.14 Output bank selector

The output bank selector (see Table 15), selects one of the four bits per display RAM address for transfer to the display register. The actual bit selected depends on the LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode: all RAM addresses of bit 0 are selected, followed sequentially by the contents of bit 1, bit 2 and then bit 3.
- In 1:3 multiplex mode: bits 0, 1 and 2 are selected sequentially.
- In 1:2 multiplex mode: bits 0 and 1 are selected.
- In the static mode: bit 0 is selected.

The PCF8566 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank select command may request the contents of bit 2 to be selected for display instead of the contents of bit 0. In 1:2 multiplex drive mode, the contents of bits 2 and 3 may be selected instead of bits 0 and 1. This enables preparation of display information in an alternative bank and the ability to switch to it once it has been assembled.

## 7.15 Input bank selector

The input bank selector loads display data into the display RAM based on the selected LCD drive configuration. Using the bank select command, display data can be loaded in bit 2 into static drive mode or in bits 2 and 3 into 1:2 multiplex drive mode. The input bank selector functions independently of the output bank selector.

## 7.16 Blinker

The display blinking capabilities of the PCF8566 are very versatile. The whole display can be blinked at frequencies selected by the blink command. The blinking frequencies are integer fractions of the clock frequency; the ratios between the clock and blinking frequencies depend on the mode in which the device is operating (see Table 7).

**Table 7. Blink frequencies**

| Blinking mode | Normal operating mode ratio | Power saving mode ratio | Blink frequency |
|---|---|---|---|
| off | - | - | blinking off |
| 1 | $f_{blink} = \frac{f_{clk}}{92160}$ | $f_{blink} = \frac{f_{elk}}{15360}$ | 2 Hz |
| 2 | $f_{blink} = \frac{f_{clk}}{184320}$ | $f_{blink} = \frac{f_{clk}}{30720}$ | 1 Hz |
| 3 | $f_{blink} = \frac{f_{clk}}{368640}$ | $f_{blink} = \frac{f_{clk}}{61440}$ | 0.5 Hz |

An additional feature is for an arbitrary selection of LCD segments to be blinked. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. Using the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blinking frequency. This mode can also be specified by the blink select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can be blinked by selectively changing the display RAM data at fixed time intervals.

If the entire display needs to be blinked at a frequency other than the nominal blinking frequency, this can be done using the mode set command to set and reset the display enable bit E at the required rate (see Table 9).

# 8. Basic architecture

## 8.1 Characteristics of the I²C-bus

The I²C-bus provides bidirectional, two-line communication between different IC or modules. The two lines are a Serial Data line (SDA) and a Serial Clock Line (SCL). When connected to the output stages of a device, both lines must be connected to a positive supply via a pull-up resistor. Data transfer is initiated only when the bus is not busy.

### 8.1.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse. Changes in the data line at this time will be interpreted as a control signal. Bit transfer is illustrated in Figure 12.

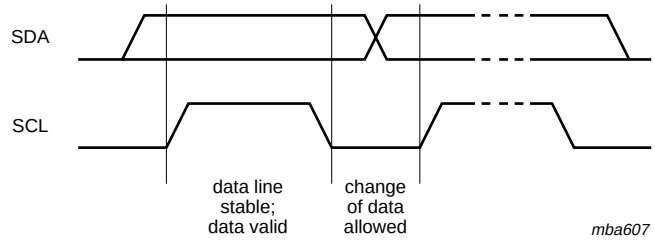



**Fig 12. Bit transfer**

#### 8.1.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Figure 13.

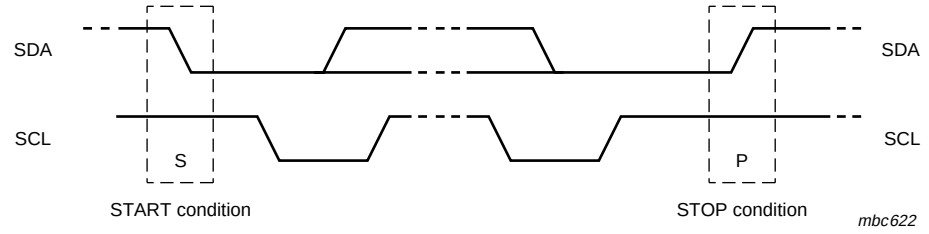



**Fig 13. Definition of START and STOP conditions**

### 8.1.2 System configuration

A device generating a message is a transmitter and a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is illustrated in Figure 14.

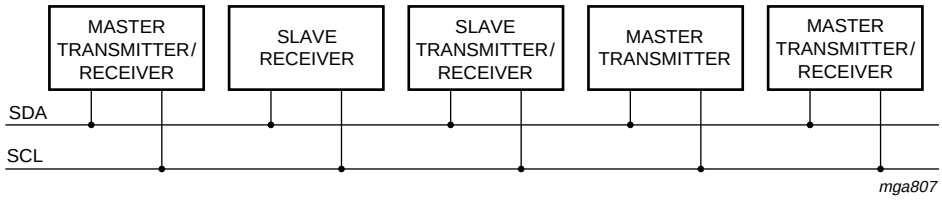



**Fig 14. System configuration**

### 8.1.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge bit. The acknowledge bit is a HIGH level signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. (See Figure 15).

Acknowledgement on the $I^2C$-bus is illustrated in

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end-of-data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the master receiver must leave the data line HIGH during the 9th pulse to not acknowledge. The master will now generate a STOP condition.

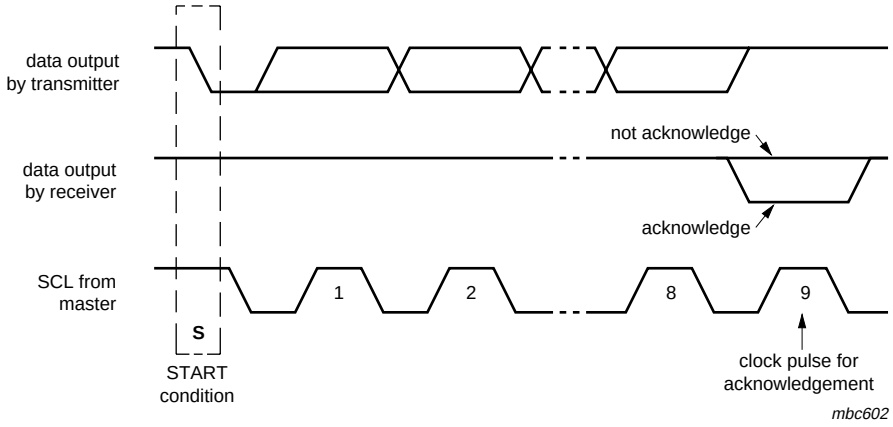



**Fig 15. Acknowledgement on the I²C-bus**

### 8.1.4 PCF8566 I²C-bus controller

The PCF8566 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8566 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, the transferred command data and the hardware subaddress.

In single device application, the hardware subaddress inputs A0, A1 and A2 are normally tied to $V_{SS}$ which defines the hardware subaddress 0. In multiple device applications A0, A1 and A2 are tied to $V_{SS}$ or $V_{DD}$ using a binary coding scheme so that no two devices with a common I²C-bus slave address have the same hardware subaddress.

In the power-saving mode it is possible that the PCF8566 is not able to keep up with the highest transmission rates when large amounts of display data are transmitted. If this situation occurs, the PCF8566 forces the SCL line LOW until its internal operations are completed. This is known as the clock synchronization feature of the I²C-bus and serves to slow down fast transmitters. Data loss does not occur.

### 8.1.5 Input filter

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

## 8.2 I²C-bus protocol

Two I²C-bus 7 bit slave addresses (0111 110 and 0111 111) are reserved for the PCF8566. The least significant bit after the slave address is bit R/$\overline{W}$. The PCF8566 is a write-only device. It will not respond to a read access, so this bit should always be logic 0. The second bit of the slave address is defined by the level tied at input SA0.

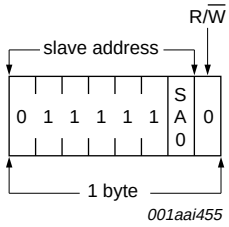



**Fig 16. Slave address structure**

Two displays controlled by PCF8566 can be recognized on the same I²C-bus which allows:

- Up to 16 PCF8566s on the same I²C-bus for very large LCD applications (see Section 13)
- The use of two types of LCD multiplex on the same I²C-bus

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the PCF8566 slave addresses. All PCF8566s with the same SA0 level acknowledge in parallel to the slave address. All PCF8566s with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, one or more command bytes (m) follow which define the status of the addressed PCF8566s. The last command byte is tagged with a cleared most significant bit, the continuation bit C. The command bytes are also acknowledged by all addressed PCF8566s on the bus.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8566 device.

The acknowledgement after each byte is made only by the (A0, A1 and A2) addressed PCF8566. After the last display byte, the I²C-bus master issues a STOP condition (P).

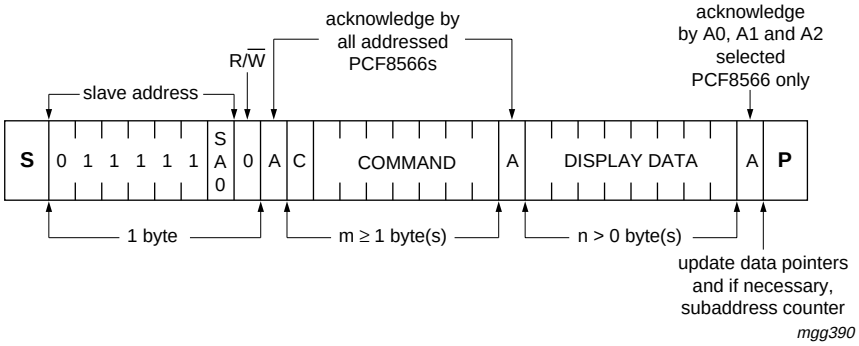
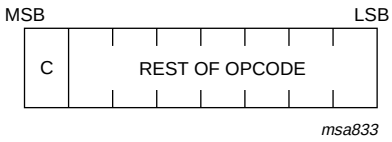



**Fig 17. I²C-bus protocol**

## 8.3 Command decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position as shown in Figure 18. When this bit is set, it indicates that the next byte of the transfer to arrive will also represent a command. If this bit is reset, it indicates that the command byte is the last in the transfer. Further bytes will be regarded as display data.

The five commands available to the PCF8566 are defined in Table 8.




(1) C = 0; last command.

(2) C = 1; commands continue.

**Fig 18. General format of byte command**

**Table 8. Definition of PCF8566 commands**

| Command | Opcode | | | | | | | | Reference | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
| Mode set | C | 1 | 0 | LP | E | B | M1 | M0 | Section 8.3.1 | defines LCD drive mode, LCD bias configuration, display status and power dissipation mode |
| Load data pointer | C | 0 | 0 | P4 | P3 | P2 | P1 | P0 | Section 8.3.2 | data pointer to define one of 24 display RAM addresses |
| Device select | C | 1 | 1 | 0 | 0 | A2 | A1 | A0 | Section 8.3.3 | define one of eight hardware subaddresses |
| Bank select | C | 1 | 1 | 1 | 1 | 0 | I | O | Section 8.3.4 | bit I: defines input bank selection (storage of arriving display data); bit O: defines output bank selection (retrieval of LCD display data) |
| Blink | C | 1 | 1 | 1 | 0 | A | BF1 | BF0 | Section 8.3.5 | defines the blink frequency and blink mode |

### 8.3.1 Mode set command

**Table 9. LCD drive mode command bit description**

| LCD drive mode | | Bit | |
|---|---|---|---|
| Drive mode | Backplane | M1 | M0 |
| static | BP0 | 0 | 1 |
| 1:2 | BP0, BP1 | 1 | 0 |
| 1:3 | BP0, BP1. BP2 | 1 | 1 |
| 1:4 | BP0, BP1. BP2, BP3 | 0 | 0 |

**Table 10. LCD bias configuration command bit description**

| LCD bias | Bit B |
|---|---|
| 1/3 bias | 0 |
| 1/2 bias | 1 |

**Table 11. Display status command bit description[1]**

| Display status | Bit E |
|---|---|
| disabled (blank) | 0 |
| enabled | 1 |

[1] The possibility to disable the display allows implementation of blinking under external control.

**Table 12. Power dissipation mode command bit description**

| Display status | Bit LP |
|---|---|
| normal mode | 0 |
| power saving mode | 1 |

### 8.3.2 Load data pointer command

**Table 13. Load data pointer command bit description**

| Description | Bit | | | | |
|---|---|---|---|---|---|
| 5 bit binary value, 0 to 23 | P4 | P3 | P2 | P1 | P0 |

### 8.3.3 Device select command

**Table 14. Device select command bit description**

| Description | Bit | | |
|---|---|---|---|
| 3 bit binary value, 0 to 7 | A2 | A1 | A0 |

### 8.3.4 Bank select command

**Table 15. Bank select command[1]**

| Bank | Mode | | Bit | Value |
|---|---|---|---|---|
| | Static | 1:2 MUX | | |
| **Input bank** | | | | |
| | RAM bit 0 | RAM bits 0 and 1 | I | 0 |
| | RAM bit 2 | RAM bits 2 and 3 | | 1 |
| **Output bank** | | | | |
| | RAM bit 0 | RAM bits 0 and 1 | O | 0 |
| | RAM bit 2 | RAM bits 2 and 3 | | 1 |

[1] The bank select command has no effect in 1:3 or 1:4 multiplex drive modes.

### 8.3.5 Blink command

**Table 16. Blink frequency command bit description**

| Blink frequency | Bit | |
|---|---|---|
| | BF1 | BF0 |
| off | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**Table 17. Blink mode command bit description**

| Blink mode | Bit A |
|---|---|
| Normal blinking | 0 |
| Alternate RAM bank blinking | 1 |

## 8.4 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8566 and coordinates their effects. The controller also loads display data into the display RAM as required by the storage order.

# 9. Internal circuitry

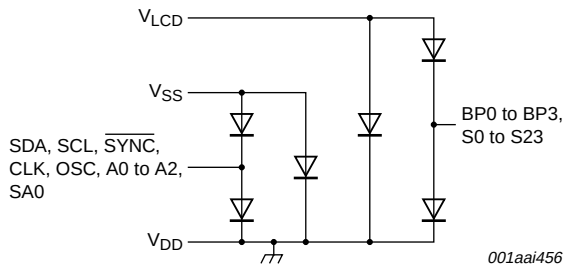



**Fig 19. Device protection diagram**

# 10. Limiting values

**CAUTION**

Static voltages across the liquid crystal display can build up when the LCD supply voltage ($V_{LCD}$) is on while the IC supply voltage ($V_{DD}$) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, $V_{LCD}$ and $V_{DD}$ must be applied or removed together.

**Table 18. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | –0.5 | 7.0 | V |
| $V_{LCD}$ | LCD supply voltage | | [1] | –0.5 | 7.0 | V |
| $V_I$ | input voltage | on each of the pins SCL, SDA, A0 to A2, OSC, CLK, $\overline{SYNC}$ and SA0 | | –0.5 | 7.0 | V |
| $V_O$ | output voltage | on each of the pins S0 to S23 and BP0 to BP3 | [1] | –0.5 | 7.0 | V |
| $I_I$ | input current | | | –20 | +20 | mA |
| $I_O$ | output current | | | –25 | +25 | mA |
| $I_{DD}$ | supply current | | | –50 | +50 | mA |
| $I_{SS}$ | ground supply current | | | –50 | +50 | mA |
| $I_{DD(LCD)}$ | LCD supply current | | | –50 | +50 | mA |
| $P_{tot}$ | total power dissipation | per package | | - | 400 | mW |
| $P_o$ | output power | | | - | 100 | mW |
| $T_{stg}$ | storage temperature | | [2] | –65 | +150 | °C |
| $V_{esd}$ | electrostatic discharge voltage | HBM | [3] | - | ±2000 | V |
| | | MM | [4] | - | ±200 | V |
| $I_{lu}$ | latch-up current | | [5] | - | 100 | mA |

[1] Values with respect to $V_{DD}$.

[2] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

[3] Pass level; Human Body Model (HBM) according to JESD22-A114.

[4] Pass level; Machine Model (MM), according to JESD22-A115.

[5] Pass level; latch-up testing, according to JESD78.

# 11. Static characteristics

**Table 19. Static characteristics**

*$V_{SS}$ = 0 V; $V_{DD}$ = 2.5 V to 6.0 V; $V_{LCD}$ = $V_{DD}$ − 2.5 V to $V_{DD}$ − 6.0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Supplies** | | | | | | | |
| $V_{DD}$ | supply voltage | | | 2.5 | - | 6.0 | V |
| $V_{LCD}$ | LCD supply voltage | | | $V_{DD}$ − 6.0 | - | $V_{DD}$ − 2.5 | V |
| $I_{DD}$ | supply current: | $f_{clk}$ = 200 kHz | [1] | - | 30 | 90 | µA |
| $I_{DD(lp)}$ | low-power mode supply current | $V_{DD}$ = 3.5 V; $V_{LCD}$ = 0 V; $f_{clk}$ = 35 kHz; A0 to A2 tied to $V_{SS}$ | [1] | - | 15 | 40 | µA |
| **Logic** | | | | | | | |
| $V_i$ | input voltage | | | $V_{SS}$ − 0.5 | - | $V_{DD}$ + 0.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | $V_{SS}$ | - | 0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | $V_{DD}$ | V |
| $I_{OL}$ | LOW-level output current | on pins CLK and $\overline{SYNC}$; $V_{OL}$ = 1.0 V; $V_{DD}$ = 5.0 V | | −1 | - | - | mA |
| $I_L$ | leakage current | on pins SA0, CLK, OSC, A0 to A2; $V_I$ = $V_{DD}$ or $V_{SS}$ | | −1 | - | +1 | µA |
| $I_{OH(CLK)}$ | HIGH-level output current on pin CLK | $V_{OH}$ = 4.0 V; $V_{DD}$ = 5.0 V | | - | - | +1 | mA |
| $I_{pd}$ | pull-down current | on pins OSC and A0 to A2; $V_I$ = 1.0 V; $V_{DD}$ = 5.0 V | | 15 | 50 | 150 | µA |
| $R_{PU}$ | pull-up resistance | on pin $\overline{SYNC}$ | | 15 | 25 | 60 | kΩ |
| $V_{POR}$ | power-on reset voltage | | [2] | - | 1.3 | 2 | V |
| $C_I$ | input capacitance | | [3] | - | - | 7 | pF |
| **$I^2C$-bus; pins SDA and SCL** | | | | | | | |
| $V_i$ | input voltage | | | $V_{SS}$ − 0.5 | - | 6 | V |
| $V_{IL}$ | LOW-level input voltage | | | $V_{SS}$ | - | 0.3$V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | 0.7$V_{DD}$ | - | 6 | V |
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | | −1 | 0 | +1 | µA |
| $I_{OL}$ | LOW-level output current | $V_{OL}$ = 0.4 V; $V_{DD}$ = 5.0 V | | −3 | - | - | mA |
| $C_I$ | input capacitance | | [3] | - | - | 7 | pF |
| $t_{w(spike)}$ | spike pulse width | on bus | | - | - | 100 | ns |

**Table 19. Static characteristics** *...continued*

*$V_{SS}$ = 0 V; $V_{DD}$ = 2.5 V to 6.0 V; $V_{LCD}$ = $V_{DD}$ − 2.5 V to $V_{DD}$ − 6.0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **LCD outputs** | | | | | | | |
| $V_{BP}$ | voltage on pin BP | BP0 to BP3; $C_{bpl}$ = 35 nF | | - | ±20 | - | mV |
| $V_S$ | voltage on pin S | S0 to S23; $C_{sgm}$ = 5 nF | | - | ±20 | - | mV |
| $Z_o$ | output impedance | on pin BP0 to BP3; $V_{LCD}$ = $V_{DD}$ − 5 V | [4] | - | 1 | 5 | kΩ |
| | | on pin S0 to S23; $V_{LCD}$ = $V_{DD}$ − 5 V | [4] | - | 3 | 7 | kΩ |

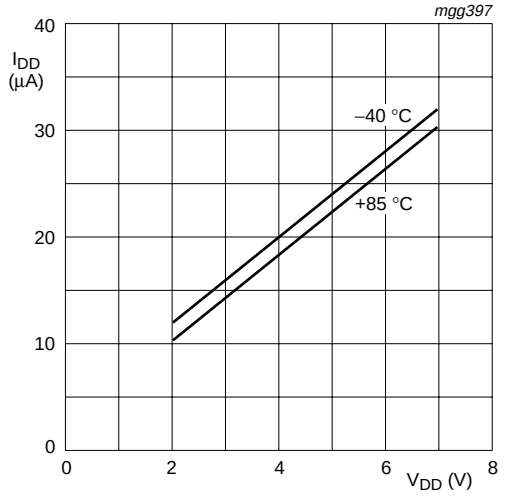
[1] Outputs open; inputs at $V_{SS}$ or $V_{DD}$; external clock with 50 % duty factor; $I^2C$-bus inactive.

[2] Resets all logic when $V_{DD}$ < $V_{POR}$.

[3] Periodically sampled, not 100 % tested.

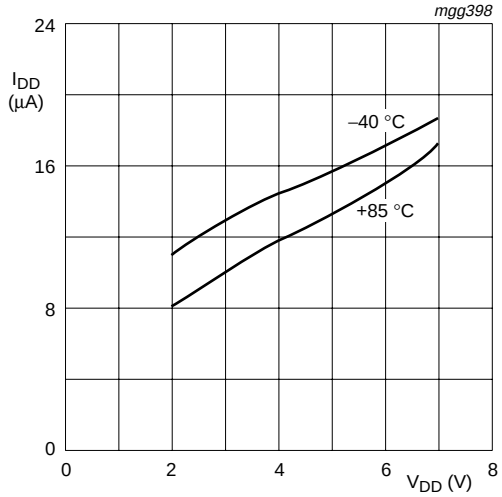
[4] Outputs measured one at a time.

## 11.1 Typical supply current characteristics




$V_{LCD}$ = 0 V; $f_{clk(ext)}$ = 200 kHz.

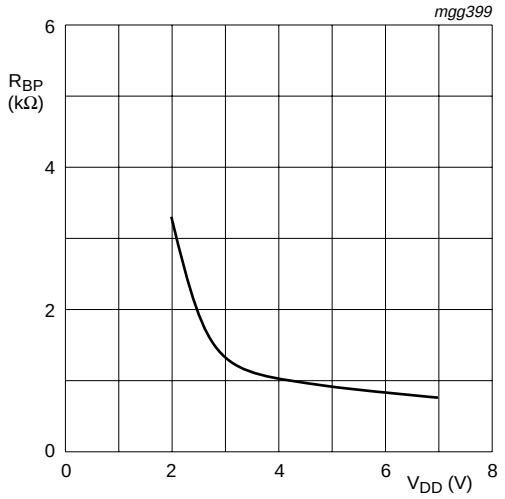
**Fig 20. Normal mode**




$V_{LCD}$ = 0 V; $f_{clk(ext)}$ = 35 kHz.

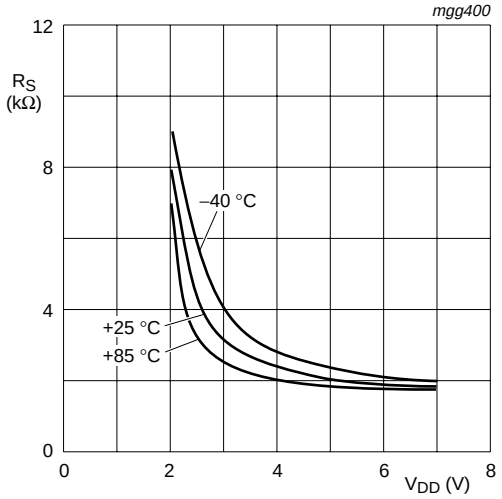
**Fig 21. Low power mode**

## 11.2 Typical LCD output characteristics




$V_{DD}$ = 5 V; $T_{amb}$ = −40 °C to +85 °C.

**Fig 22. Backplane output impedance BP0 to BP3 ($R_{BP}$)**




$V_{DD}$ = 5 V.

**Fig 23. Segment output impedance S0 to S23 ($R_S$)**

# 12. Dynamic characteristics

**Table 20. Dynamic characteristics**

*$V_{SS}$ = 0 V; $V_{DD}$ = 2.5 V to 6.0 V; $V_{LCD}$ = $V_{DD}$ − 2.5 V to $V_{DD}$ − 6.0 V; $T_{amb}$ = −40 °C to +85 °C; unless otherwise specified.* [1]

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Clock** | | | | | | | |
| $f_{clk}$ | clock frequency | normal mode; $V_{DD}$ = 5 V | [2] | 125 | 200 | 315 | kHz |
| | | power saving mode; $V_{DD}$ = 3.5 V | | 21 | 31 | 48 | kHz |
| $t_{clk(H)}$ | HIGH-level clock time | | | 1 | - | - | µs |
| $t_{clk(L)}$ | LOW-level clock time | | | 1 | - | - | µs |
| $t_{PD(SYNC\_N)}$ | $\overline{SYNC}$ propagation delay | | | - | - | 400 | ns |
| $t_{SYNC\_NL}$ | $\overline{SYNC}$ LOW time | | | 1 | - | - | µs |
| $t_{PD(drv)}$ | driver propagation delay | with test loads; $V_{LCD}$ = $V_{DD}$ − 5 V | | - | - | 30 | µs |
| **I²C-bus** | | | | | | | |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 4.7 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 4.0 | - | - | µs |
| $t_{LOW}$ | low period of the SCL clock | | | 4.7 | - | - | µs |
| $t_{HIGH}$ | high period of the SCL clock | | | 4.0 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 4.7 | - | - | µs |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | - | ns |
| $t_{SU;DAT}$ | data set-up time | | | 250 | - | - | ns |
| $t_r$ | rise time of both SDA and SCL signals | | | - | - | 1.0 | µs |
| $t_f$ | fall time of both SDA and SCL signals | | | - | - | 300 | ns |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 4.7 | - | - | µs |

[1] All timing values referred to $V_{IH}$ and $V_{IL}$ levels with an input voltage swing of $V_{SS}$ to $V_{DD}$.

[2] At $f_{clk}$ < 125 kHz, I²C-bus maximum transmission speed is derated.

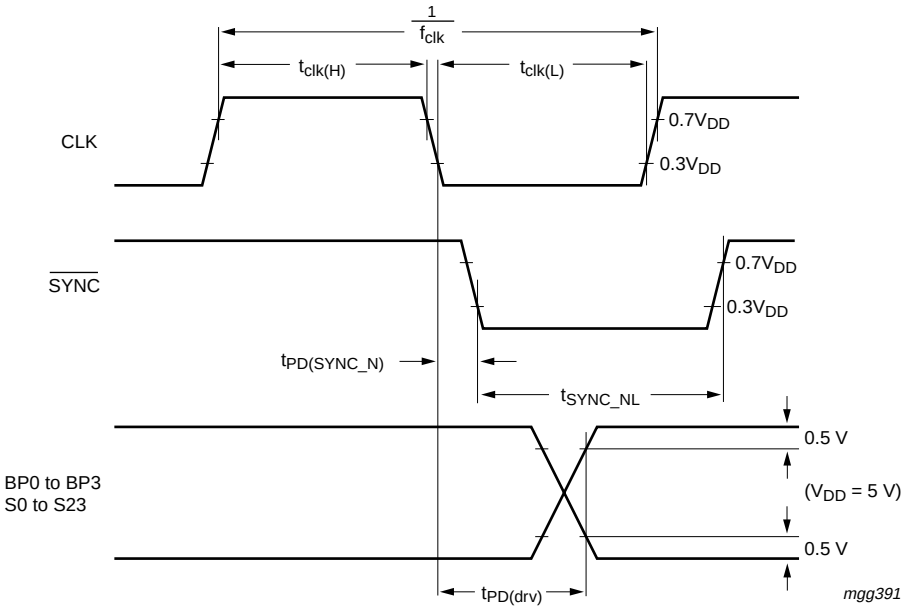



**Fig 24. Driver timing waveforms**

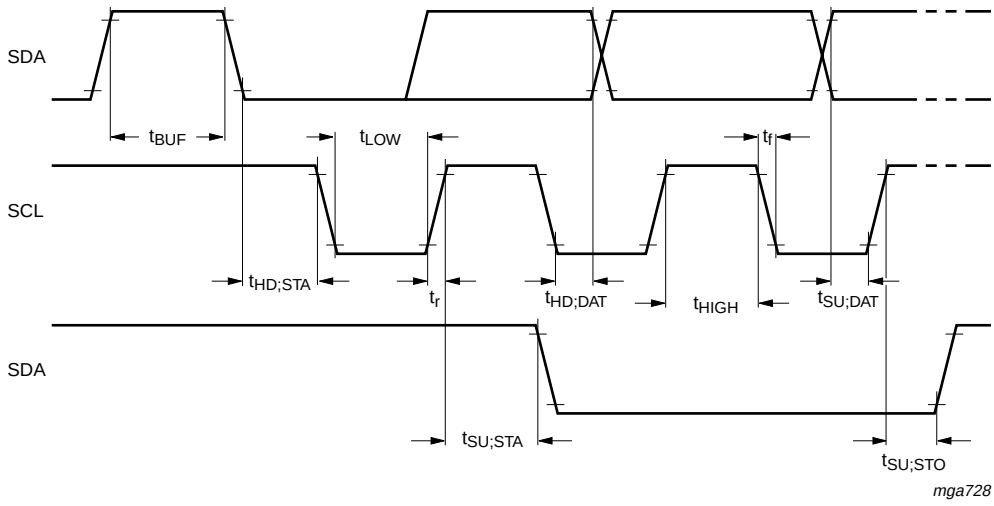



**Fig 25. $I^2C$-bus timing waveforms**

# 13. Application information

## 13.1 Cascaded operation

Large display configurations of up to sixteen PCF8566s can be recognized on the same $I^2C$-bus by using the 3-bit hardware subaddress (A0, A1 and A2) and the programmable $I^2C$-bus slave address (SA0).

**Table 21. Addressing cascaded PCF8566**

| Cluster | Bit SA0 | Pin A2 | Pin A1 | Pin A0 | Device |
|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 |
| | | 0 | 0 | 1 | 1 |
| | | 0 | 1 | 0 | 2 |
| | | 0 | 1 | 1 | 3 |
| | | 1 | 0 | 0 | 4 |
| | | 1 | 0 | 1 | 5 |
| | | 1 | 1 | 0 | 6 |
| | | 1 | 1 | 1 | 7 |
| 2 | 1 | 0 | 0 | 0 | 8 |
| | | 0 | 0 | 1 | 9 |
| | | 0 | 1 | 0 | 10 |
| | | 0 | 1 | 1 | 11 |
| | | 1 | 0 | 0 | 12 |
| | | 1 | 0 | 1 | 13 |
| | | 1 | 1 | 0 | 14 |
| | | 1 | 1 | 1 | 15 |

Cascaded PCF8566s are synchronized. They can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8566s of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 26).

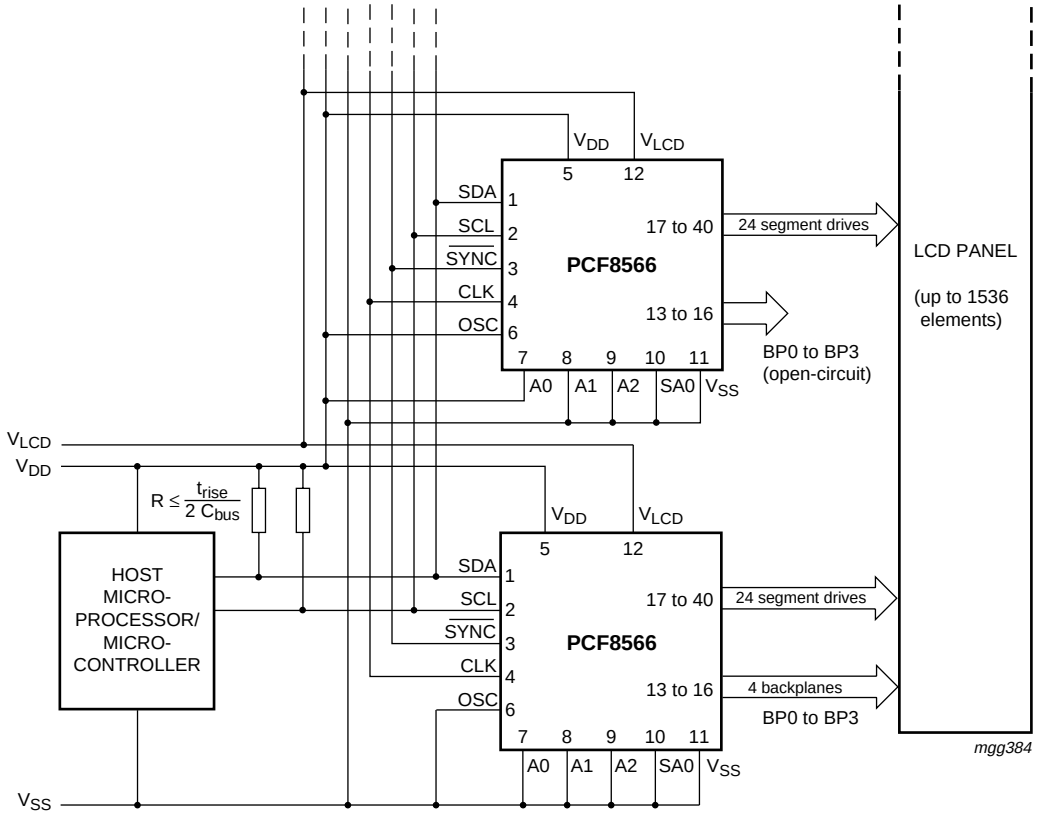



**Fig 26. Cascaded PCF8566 configuration**

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8566s. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments or by defining a multiplex mode when PCF8566s with differing SA0 levels are cascaded).

$\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8566 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. If synchronization in the cascade is lost, it is restored by the first PCF8566 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8566 are shown in Figure 27.

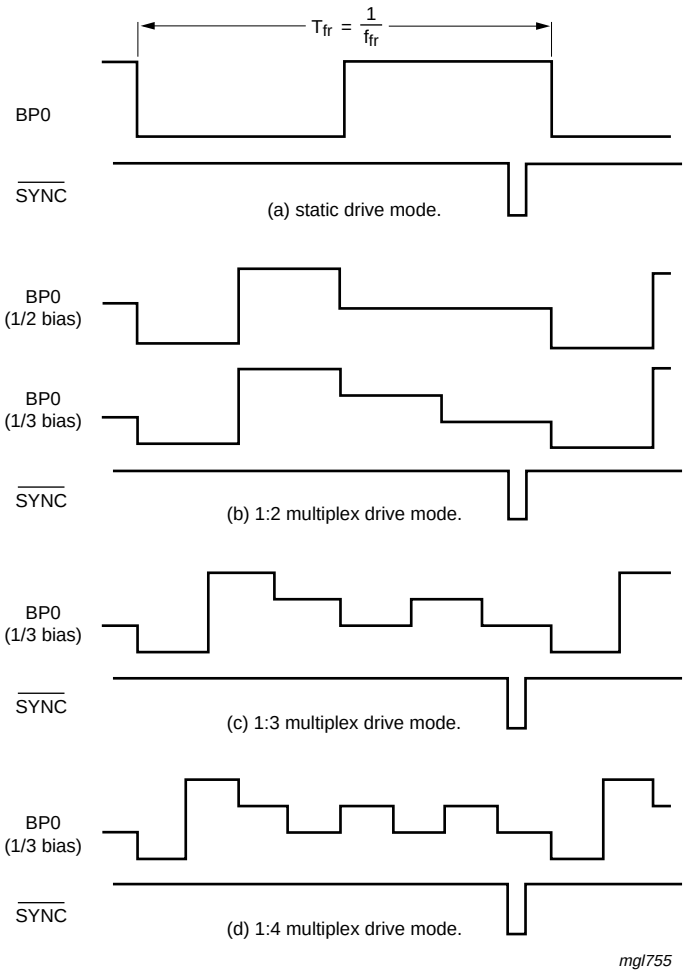



**Fig 27. Synchronization of the cascade for the various PCF8566 drive modes**

Single plane wiring of packaged PCF8566s is illustrated in Figure 28.

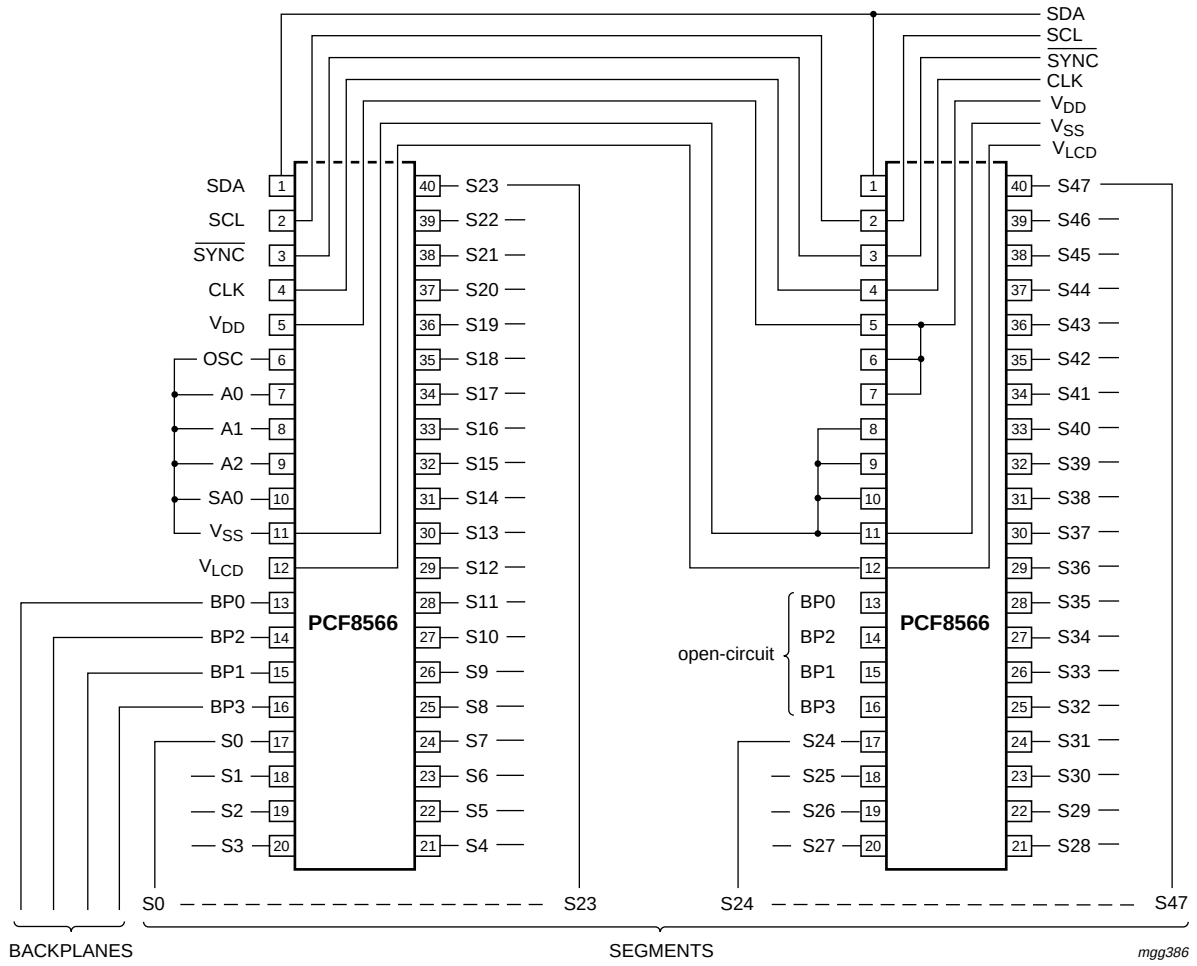
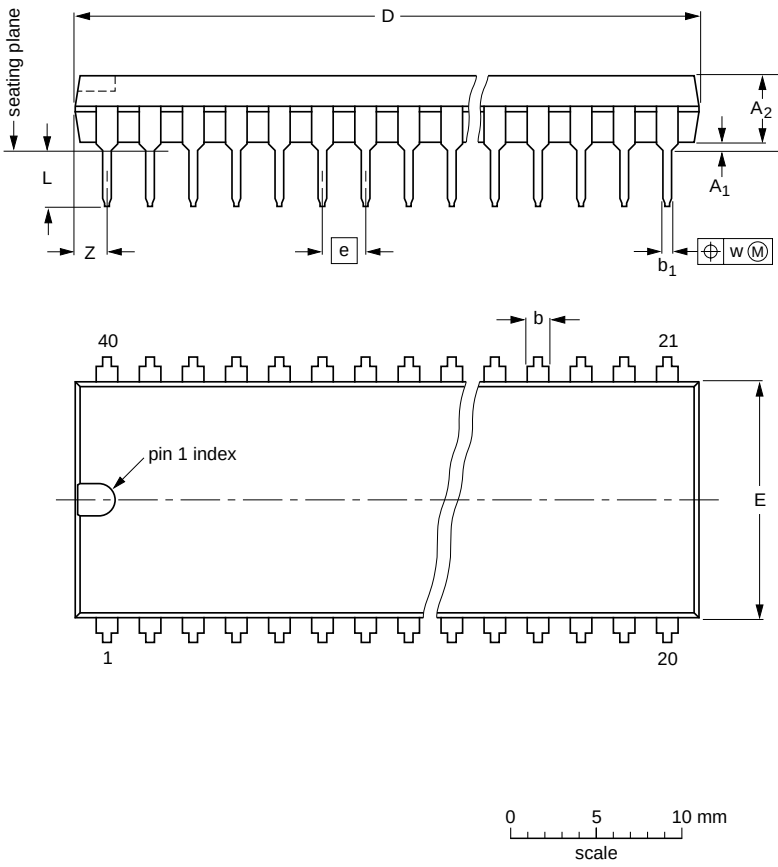



**Fig 28. Single plane wiring of packaged PCF8566s**

# 14. Package outline

**DIP40: plastic dual in-line package; 40 leads (600 mil)** **SOT129-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7 | 0.51 | 4 | 1.70<br>1.14 | 0.53<br>0.38 | 0.36<br>0.23 | 52.5<br>51.5 | 14.1<br>13.7 | 2.54 | 15.24 | 3.60<br>3.05 | 15.80<br>15.24 | 17.42<br>15.90 | 0.254 | 2.25 |
| inches | 0.19 | 0.02 | 0.16 | 0.067<br>0.045 | 0.021<br>0.015 | 0.014<br>0.009 | 2.067<br>2.028 | 0.56<br>0.54 | 0.1 | 0.6 | 0.14<br>0.12 | 0.62<br>0.60 | 0.69<br>0.63 | 0.01 | 0.089 |

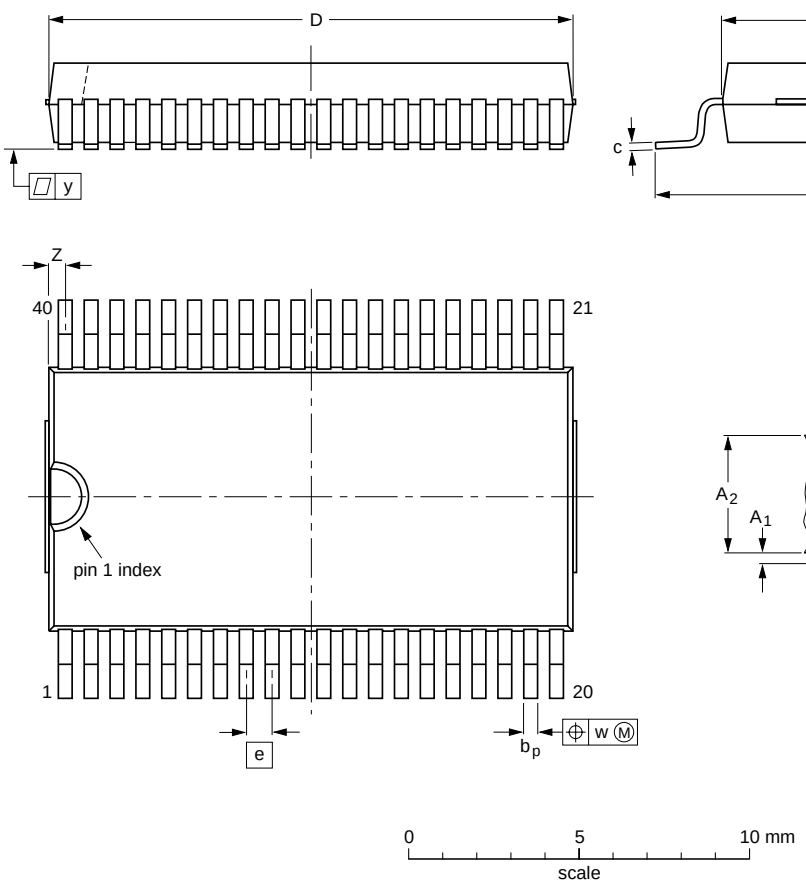
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT129-1 | 051G08 | MO-015 | SC-511-40 | | | ~~99-12-27~~<br>03-02-13 |

**Fig 29. Package outline SOT129-1 (DIP40)**

**VSO40: plastic very small outline package; 40 leads** **SOT158-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.7 | 0.3<br>0.1 | 2.45<br>2.25 | 0.25 | 0.42<br>0.30 | 0.22<br>0.14 | 15.6<br>15.2 | 7.6<br>7.5 | 0.762 | 12.3<br>11.8 | 2.25 | 1.7<br>1.5 | 1.15<br>1.05 | 0.2 | 0.1 | 0.1 | 0.6<br>0.3 | $7^o$<br>$0^o$ |
| inches | 0.11 | 0.012<br>0.004 | 0.096<br>0.089 | 0.01 | 0.017<br>0.012 | 0.0087<br>0.0055 | 0.61<br>0.60 | 0.30<br>0.29 | 0.03 | 0.48<br>0.46 | 0.089 | 0.067<br>0.059 | 0.045<br>0.041 | 0.008 | 0.004 | 0.004 | 0.024<br>0.012 | |

**Notes**

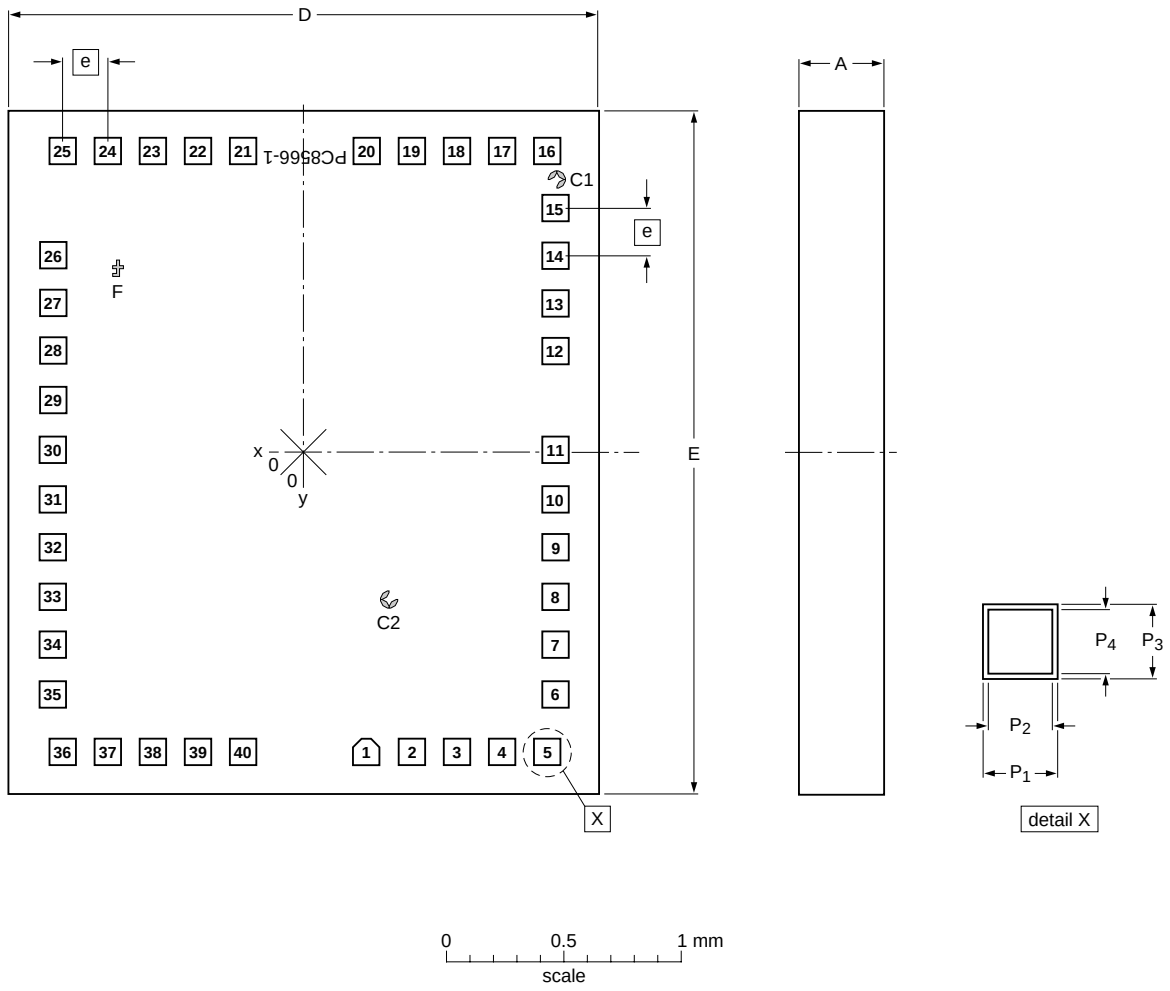
1. Plastic or metal protrusions of 0.4 mm (0.016 inch) maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT158-1 | | | | | | ~~95-01-24~~<br>03-02-19 |

**Fig 30. Package outline SOT158-1 (VSO40)**

## 15. Bare die outline

**Wire bond die; 40 bonding pads; 2.5 x 2.91 x 0.381 mm** **PCF8566U**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | | A | D | E | e | $P_1$(1) | $P_2$(2) | $P_3$(1) | $P_4$(2) |
|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.406 | 2.5 | 2.91 | 0.548 | 0.12 | 0.106 | 0.12 | 0.106 |
| | nom | 0.381 | | | 0.200 | | | | |
| | min | 0.356 | | | 0.018 | | | | |

**Notes**
1. Pad size
2. Passivation opening

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| PCF8566U | | | | | | ~~08-06-19~~ 08-09-03 |

**Fig 31. Bare die outline PCF8566U**

**Table 22. Bonding pad description**

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 31).*

| Symbol | Pad | X (μm) | Y (μm) | Description |
|---|---|---|---|---|
| SDA | 1 | 200 | −1235 | $I^2C$-bus data input / output |
| SCL | 2 | 400 | −1235 | $I^2C$-bus clock input / output |
| $\overline{SYNC}$ | 3 | 604 | −1235 | cascade synchronization input / output |
| CLK | 4 | 856 | −1235 | external clock input / output |
| $V_{DD}$ | 5 | 1062 | −1235 | supply voltage |
| OSC | 6 | 1080 | −1235 | oscillator select |
| A0 | 7 | 1080 | −825 | $I^2C$-bus subaddress input |
| A1 | 8 | 1080 | −625 | |
| A2 | 9 | 1080 | −425 | |
| SA0 | 10 | 1080 | −225 | $I^2C$-bus slave address bit 0 input |
| $V_{SS}$ | 11 | 1080 | −25 | logic ground |
| $V_{LCD}$ | 12 | 1080 | 347 | LCD supply voltage |
| BP0 | 13 | 1080 | 547 | LCD backplane output |
| BP2 | 14 | 1080 | 747 | |
| BP1 | 15 | 1080 | 947 | |
| BP3 | 16 | 1074 | 1235 | |
| S0 | 17 | 874 | 1235 | LCD segment output |
| S1 | 18 | 674 | 1235 | |
| S2 | 19 | 474 | 1235 | |
| S3 | 20 | 274 | 1235 | |
| S4 | 21 | −274 | 1235 | |
| S5 | 22 | −474 | 1235 | |
| S6 | 23 | −674 | 1235 | |
| S7 | 24 | −874 | 1235 | |
| S8 | 25 | −1074 | 1235 | |
| S9 | 26 | −1080 | 765 | |
| S10 | 27 | −1080 | 565 | |
| S11 | 28 | −1080 | 365 | |
| S12 | 29 | −1080 | 165 | |
| S13 | 30 | −1080 | −35 | |
| S14 | 31 | −1080 | −235 | |
| S15 | 32 | −1080 | −435 | |
| S16 | 33 | −1080 | −635 | |
| S17 | 34 | −1080 | −835 | |
| S18 | 35 | −1080 | −1035 | |
| S19 | 36 | −1056 | −1235 | |
| S20 | 37 | −830 | −1235 | |

**Table 22. Bonding pad description** *…continued*

*All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip (see Figure 31).*

| Symbol | Pad | X (μm) | Y (μm) | Description |
|---|---|---|---|---|
| S21 | 38 | –630 | –1235 | |
| S22 | 39 | –430 | –1235 | |
| S23 | 40 | –230 | –1235 | |

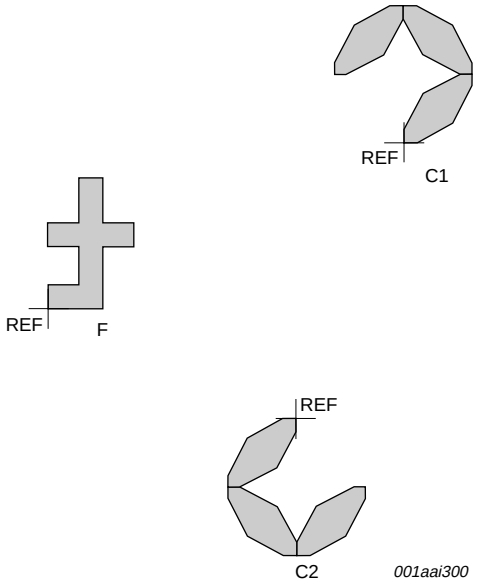



**Fig 32. Alignment marks**

**Table 23. Alignment marks**

| Symbol | X (μm) | Y (μm) |
|---|---|---|
| C1 | 1100 | 1090 |
| C2 | 325 | –625 |
| F | –790 | 700 |

## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 17. Packing information

Tray information for the PCF8566U is shown in Figure 33, Figure 35 and Table 24.

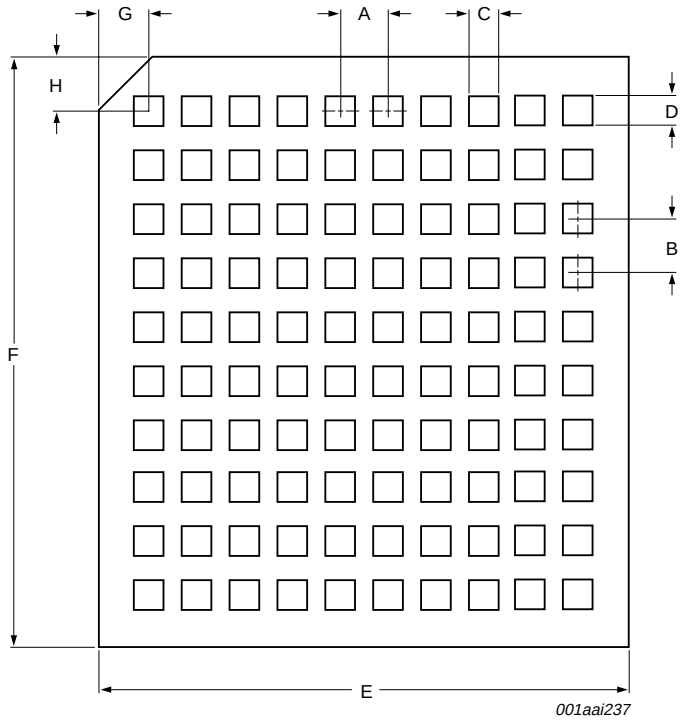



Fig 33. Tray details

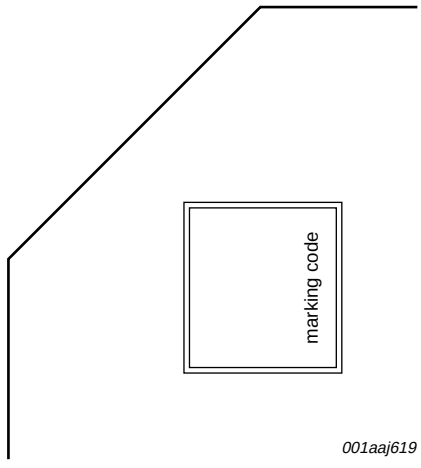



Fig 34. Tray alignment

Table 24. Tray dimensions

| Symbol | Description | Value |
|---|---|---|
| A | pocket pitch; x direction | 4.43 mm |
| B | pocket pitch; y direction | 4.43 mm |
| C | pocket width; x direction | 3.04 mm |
| D | pocket width; y direction | 3.04 mm |

**Table 24. Tray dimensions** *…continued*

| Symbol | Description | Value |
|---|---|---|
| E | tray width; x direction | 50.8 mm |
| F | tray width; y direction | 50.8 mm |
| G | cut corner to pocket 1,1 center | 5.47 mm |
| H | cut corner to pocket 1,1 center | 5.47 mm |
| x | number of pockets; x direction | 10 |
| y | number of pockets; y direction | 10 |

# 18. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 18.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 18.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair

- Lead-free soldering versus SnPb soldering

## 18.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 18.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 35) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 25 and 26

**Table 25. SnPb eutectic process (from J-STD-020C)**

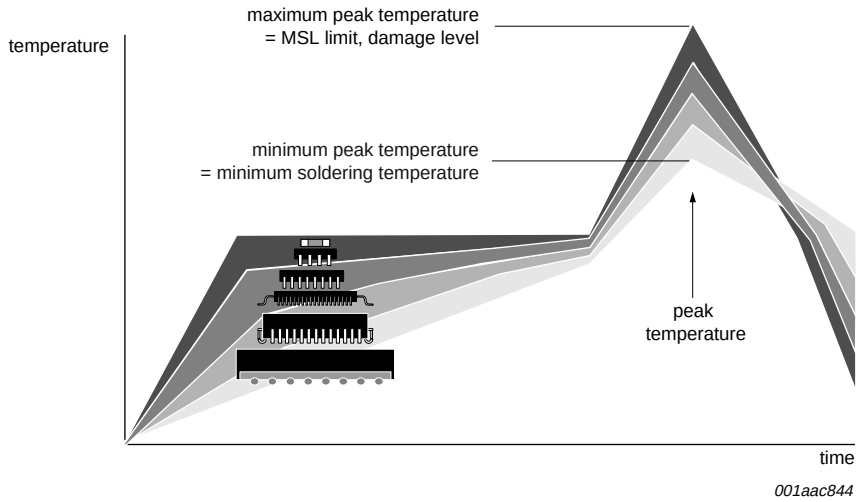
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 26. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 35.




MSL: Moisture Sensitivity Level

**Fig 35. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 19. Abbreviations

**Table 27. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DC | Direct Current |
| HBM | Human Body Model |
| $I^2C$ | Inter-Integrated Circuit |
| IC | Integrated Circuit |
| LCD | Liquid Crystal Display |
| MM | Machine Model |
| MSL | Moisture Sensitivity Level |
| POR | Power-On Reset |
| RC | Resistance and Capacitance |
| RAM | Random Access Memory |
| RMS | Root Mean Square |
| SMD | Surface Mount Device |
| TTL | Transistor-Transistor Logic |

## 20. Revision history

**Table 28. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCF8566_7 | 20090225 | Product data sheet | - | PCF8566_6 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Added U and TS type<br>• Added tray information<br>• Changed values in limiting values table from relative to absolute values<br>• Changed letter symbols to NXP approved symbols<br>• Rewritten chapter 7.3 | | | |
| PCF8566_6 | 19980504 | Product specification | - | PCF8566_5 |
| PCF8566_5 | 19970402 | Product specification | - | PCF8566_4 |
| PCF8566_4 | 19961203 | Product specification | - | PCF8566_3 |
| PCF8566_3 | 19961029 | Product specification | - | PCF8566_2 |

# 21. Legal information

## 21.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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