

# Samurai-6M/MX

6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996MX - Green Package Version)

ADM6996M/MX, Version AD

Data Sheet

Revision 1.4

Communication Solutions



Never stop thinking

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**ADM6996M/MX, 6 Port 10/100 Mbit/s Single Chip Ethernet Switch Controller (ADM6996MX - Green Package Version)**

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## 1 Product Overview

### 1.1 Samurai-6M/6MX (ADM6996M/MX) Overview

The Samurai-6M/6MX (ADM6996M/MX) is a high performance, low cost, highly integrated (Controller, PHY and Memory) four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSSI/RMII. The Samurai-6M/6MX (ADM6996M/MX) is intended for applications such as stand alone bridges for the low cost SOHO markets such as 5-port switches and router applications. The Samurai-6MX (ADM6996MX) is the environmentally friendly “green” package version.

**The Samurai-6M/6MX (ADM6996M/MX) provides functions such as:** 802.1p(Q.O.S.), 802.1Q(VLAN), Port MAC address locking, management, port status, TP auto-MDIX, 25M crystal & extra MII port functions to meet customer requests on switch demand.

The Samurai-6M/6MX (ADM6996M/MX) also supports back pressure in Half-Duplex mode and the 802.3x Flow Control Pause packet in Full-Duplex mode to prevent packet loss when buffers are full. When Back Pressure is enabled, and there is no receive buffer available for the incoming packet, the Samurai-6M/6MX (ADM6996M/MX) will issue a JAM pattern on the receiving port in Half Duplex mode and issue the 802.3x Pause packet back to the receiving end in Full Duplex mode.

The built-in SRAM used for the packet buffer is divided into 256 bytes per block to achieve the optimized memory utilization through complicated link lists on packets with various lengths.

The Samurai-6M/6MX (ADM6996M/MX) also supports priority features using Port-Based, VLAN and IP TOS field checking. Users can easily set different priority modes in individual ports, through a small low-cost micro controller when initializing or configuring on-the-fly. Each output port supports four queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packets such as Voice, Video and Data. 802.1Q, Tag/Untag, and up to 16 groups of VLAN are also supported.

An intelligent address recognition algorithm allows Samurai-6M/6MX (ADM6996M/MX) to recognize up to 2K different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by Samurai-6M/6MX (ADM6996M/MX) to use on building Internet access to prevent multiple users sharing one port.

### 1.2 Features

- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces and two MII port with one MII supporting GPSSI/RMII
- Supports four 10M/100M auto-detect Half/Full duplex switch ports with TX/FX interfaces, one MII port (for CPU LAN MII) and one isolated PHY(for CPU WAN MII).Five 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces
- 2K MAC address tables with 4-ways associative hash algorithm
- 6KX64 bits packet buffers are divided into 192 blocks of 256 bytes each
- Four queues for QoS
- Priority features by Port-Based, 802.1p, IP TOS, Diffserv, TCP/UDP Port Application-Based of packets
- Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed
- Single/Dual color LED mode with Power On auto diagnostic. Collision/Duplex LED can be separated using register setting
- 802.3x Flow Control pause packet for Full Duplex
- Back Pressure function for Half Duplex operation
- Supports packet lengths up to 1518/1522 (Default)/1536/1784 bytes in maximum
- Scalable Per Port Bandwidth Control (Both Ingress and Egress).
- Broadcast/Multicast Storm Suppression

- 802.1Q VLAN. Up to 16 VLAN groups are implemented by full 12 bits VID matching
- MAC clone function to enable multiple WAN application
- TP interface Auto MDIX function for auto TX/RX swap by strapping-pin.
- Interrupt pin, Interrupt Register and Interrupt Mask Register. Programmable interrupt polarity (Default active low)
- Easy Management 32-bit smart counter for per port RX/TX byte/packet count, 16-bit smart counter for per port ERROR count and Collision count
- Supports 32 hardware IGMP Table (Multicast Table)
- MAC Address Table is accessible
- Supports 802.1x security function
- Supports Spanning Tree Protocol
- Supports internal counter/PHY status output for management system
- 25M Crystal
- 128 QFP package with 0.18  $\mu\text{m}$  technology. 1.8 V/3.3 V power supply.
- 1.0 W low power consumption.

### **1.3 Applications**

Samurai-6M/6MX (ADM6996M/MX):

- SOHO 5-port switch
- 5-port switch + Router with 2 MII CPU interface

## 1.4 Block Diagram

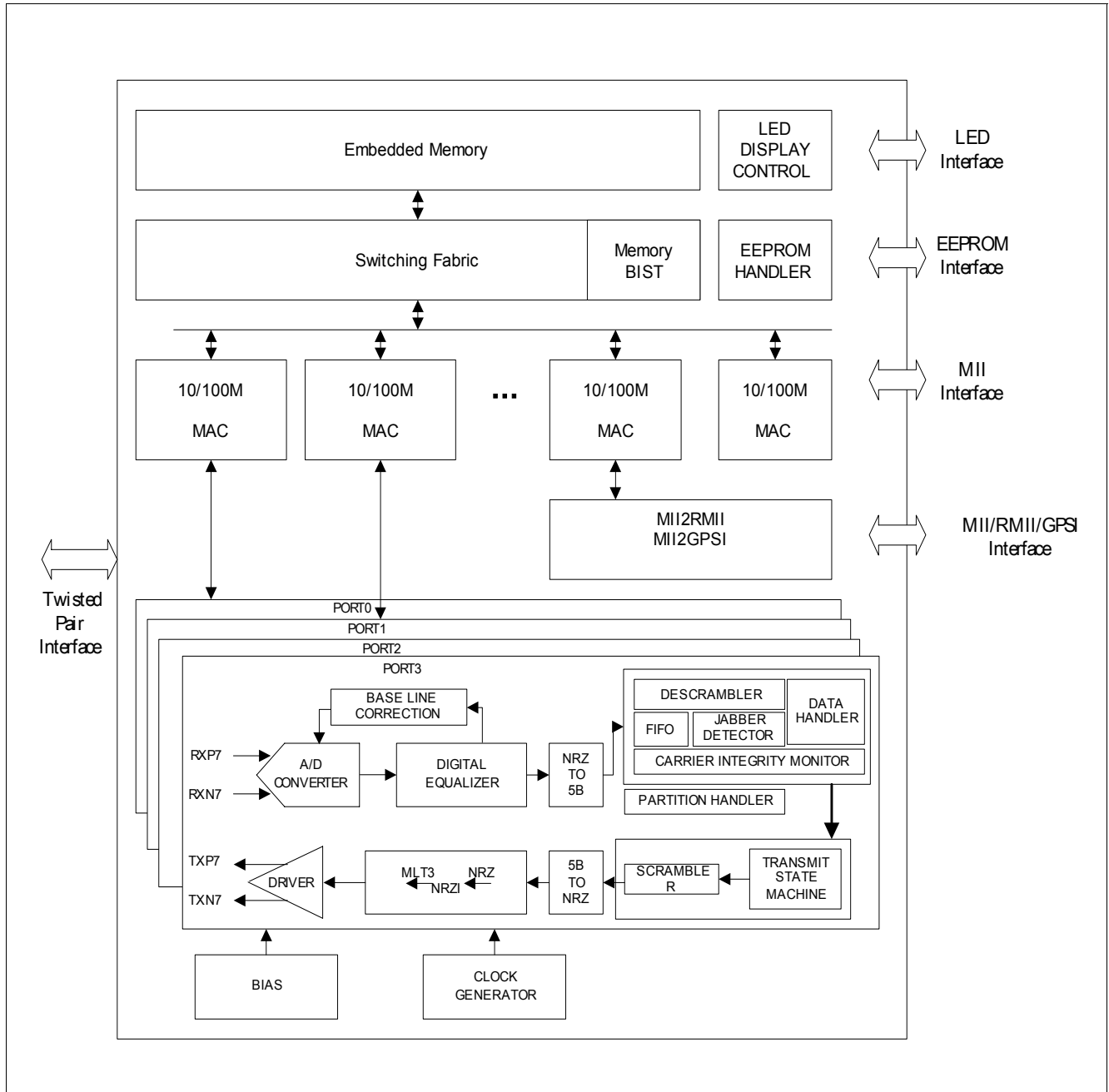


Figure 1 Samurai-6M/6MX (ADM6996M/MX) Block Diagram

## 1.5 Data Lengths

- qword: 64 bits
- dword: 32 bits
- word: 16 bits
- byte: 8 bits
- nibble: 4 bits

## 2 Interface Description

This chapter describes the interface descriptions for the Samurai-6M/6MX (ADM6996M/MX)

- Pin Diagram
- Abbreviations
- Pin Description by Function

### 2.1 Pin Diagram

Figure 2 shows the pin diagram for the Samurai-6M/6MX (ADM6996M/MX).

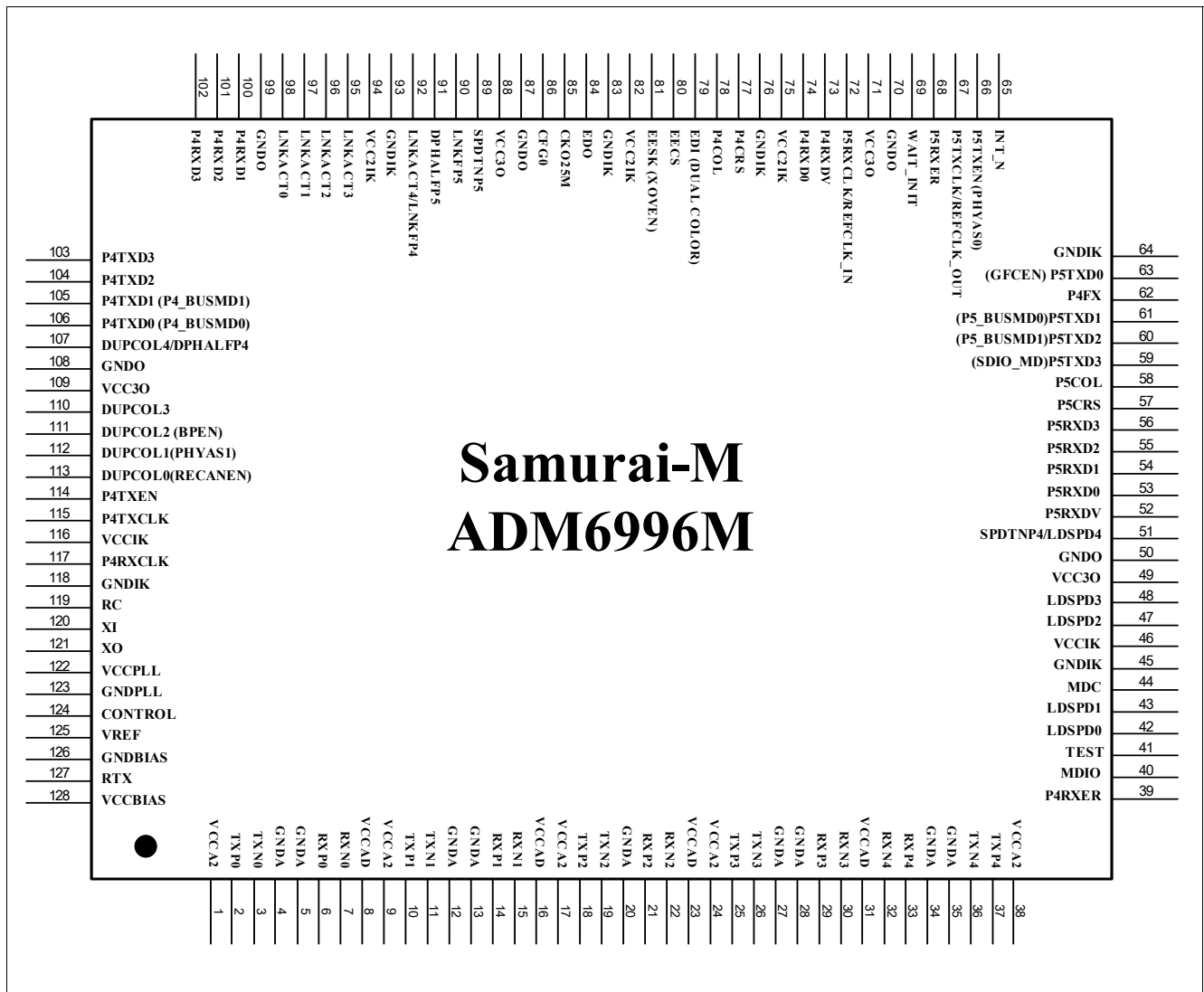


Figure 2 4 TP/FX PORT + 2 MII PORT 128 Pin Diagram

## 2.2 Abbreviations

Standard abbreviations for I/O tables:

**Table 1 Abbreviations for Pin Type**

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

**Table 2 Abbreviations for Buffer Type**

Abbreviations	Description
Z	High impedance
PU	Pull up, 10 k $\Omega$
PD	Pull down, 10 k $\Omega$
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

## 2.3 Pin Description by Function

**Samurai-6M/6MX (ADM6996M/MX) pins are categorized into one of the following groups:**

- Network Media Connection
- Port 4 MII Interface
- Port 5 MII Interface
- LED Interface
- EEPROM Interface
- Power/Ground, 48 pins
- Miscellaneous

Note: [Table 1](#) can be used for reference.

**Table 3 IO Signals**

Ball No.	Name	Pin Type	Buffer Type	Function
<b>Network Media Connection</b>				
33	RXP_4	AI/O	ANA	<b>Receive Pair</b> Differential data is received on this pin.
29	RXP_3			
21	RXP_2			
14	RXP_1			
6	RXP_0			
32	RXN_4	AI/O	ANA	
30	RXN_3			
22	RXN_2			
15	RXN_1			
7	RXN_0			
37	TXP_4	AI/O	ANA	<b>Transmit Pair</b> Differential data is transmitted on this pin.
25	TXP_3			
18	TXP_2			
10	TXP_1			
2	TXP_0			
36	TXN_4	AI/O	ANA	
26	TXN_3			
19	TXN_2			
11	TXN_1			
3	TXN_0			
<b>Port 4 MII Interface</b>				
74	MMII_P4RXD0	I	PD, LVTTTL	<b>Port 4 Receive Data Bit 0 in MAC MII Mode</b> In MAC MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD0	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Data Bit 0 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, the bit is the LSB of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
102	MMII_P4RXD3	I	PD, LVTTTL	<b>Port 4 Receive Data Bit 3 in MAC MII Mode</b> In MAC MII mode, this bit is bit[3] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD3	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Data Bit 3 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[3] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
101	MMII_P4RXD2	I	PD, LVTTTL	<b>Port 4 Receive Data Bit 2 in MAC MII Mode</b> In MAC MII mode, this pin is bit[2] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD2	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Data Bit 2 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[2] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
100	MMII_P4RXD1	I	PD, LVTTTL	<b>Port 4 Receive Data Bit 1 in MAC MII Mode</b> In MAC MII mode, this pin is bit[1] of MII receive data, and synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXD1	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Data Bit 1 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[1] of MII receive data output and synchronous to the rising edge of PMII_P4RXCLK.
73	MMII_P4RXDV	I	PD, LVTTTL	<b>Port 4 Receive Data Valid in MAC MII Mode</b> Active high to indicate that the data on MMII_P4RXD[3:0] is valid. Synchronous to the rising edge of MMII_P4RXCLK.
	PMII_P4RXDV	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Data Valid in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is an active high output signal to indicate PMII_P4RXD[3:0] is valid. Synchronous to the rising edge of PMII_P4RXCLK.
39	MII_P4RXER	I	PD, LVTTTL	<b>Port 4 Receive Error in MAC MII Mode</b> Active high to indicate that there is symbol error on the MII_P4RXD[3:0]. Only valid in 100M operation.
77	MMII_P4CRS	I	PD, LVTTTL	<b>Port 4 Carrier Sense in MAC MII Mode</b> In full duplex mode, MMII_P4CRS reflects the receive carrier sense situation on medium only; In Half Duplex, CRS will be high both in receive and transmit condition.
	PMII_P4CRS	O	8 mA, PD, LVTTTL	<b>Port 4 Carrier Sense in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is used to output Carrier Sense status.
78	MMII_P4COL	I	PD, LVTTTL	<b>Port 4 Collision input in MAC MII Mode</b> Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	PMII_P4COL	O	8 mA, PD, LVTTTL	<b>Port 4 Collision output in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is used to output collision status.



**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
106	P4_BUSMD0	I	PD, LVTTTL	<b>Port 4 Bus Type Configuration 0</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) for Port 4 Configuration Bit 0. Combined with <b>CFG0</b> and <b>P4_BUSMD1</b> , Samurai-6M/6MX (ADM6996M/MX) provides 4 bus type for port 4. See <b>CFG0</b> pin description for more details. <i>Note: Power On Setting</i>
	MMII_P4TXD0	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Data Bit 0 in MAC MII Mode</b> The LSB bit of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD0	I	PD, LVTTTL	<b>Port 4 Transmit Data Bit 0 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is the LSB of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
105	P4_BUSMD1	I	PD, LVTTTL	<b>Port 4 Bus Type Configuration 1</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) for Port 4 Configuration Bit 1. Combined with <b>CFG0</b> and <b>P4_BUSMD0</b> , Samurai-6M/6MX (ADM6996M/MX) provides 4 bus type for port 4. See <b>CFG0</b> for more details. <i>Note: Power On Setting</i>
	MMII_P4TXD1	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Data Bit 1 in MAC MII Mode</b> The bit[1] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD1	I	PD, LVTTTL	<b>Port 4 Transmit Data Bit 1 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[1] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
103	MMII_P4TXD3	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Data Bit 3 in MAC MII Mode</b> The bit[3] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD3	I	PD, LVTTTL	<b>Port 4 Transmit Data Bit 3 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[3] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.
104	MMII_P4TXD2	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Data Bit 2 in MAC MII Mode</b> The bit[2] of MAC MII Transmit data of port 4. Synchronous to the rising edge of MMII_P4TXCLK.
	PMII_P4TXD2	I	PD, LVTTTL	<b>Port 4 Transmit Data Bit 2 in PCS MII Mode</b> When port 4 is operating in PCS MII mode, this pin is bit[2] of MII transmit data input and synchronous to the rising edge of PMII_P4TXCLK.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
114	MMII_P4TXEN	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Enable in MAC MII Mode</b> Output by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of MMII_P4TXCLK when Samurai-6M/6MX (ADM6996M/MX) is programmed to MAC Type MII.
	PMII_P4TXEN	I	PD, LVTTTL	<b>Port 4 Transmit Enable in PCS MII Mode</b> It is the MII Transmit Enable input to Samurai-6M/6MX (ADM6996M/MX) when programmed to PCS Type MII.
117	MMII_P4RXCLK	I	PD, LVTTTL	<b>Port 4 Receive Clock in MAC MII Mode</b> 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. MMII_P4RXDV and MMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4RXCLK	O	8 mA, PD, LVTTTL	<b>Port 4 Receive Clock in PCS MII Mode</b> 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. PMII_P4RXDV and PMII_P4RXD[3:0] should be synchronous to the rising edge of this clock
115	MMII_P4TXCLK	I	PD, LVTTTL	<b>Port 4 Transmit Clock in MAC MII Mode</b> 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. MMII_P4TXEN and MMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
	PMII_P4TXCLK	O	8 mA, PD, LVTTTL	<b>Port 4 Transmit Clock in PCS MII Mode</b> 25MHz Free Running clock in 100M Mode and 2.5 MHz free running clock in 10M Mode. PMII_P4TXEN and PMII_P4TXD[3:0] should be synchronous to the rising edge of this clock
62	P4FX	I	PD, LVTTTL	<b>Port 4 Fiber Selection for PCS MII/PHY mode</b> During power on reset, value will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) as port 4 Fiber select. 0 <sub>B</sub> Twisted Pair Mode 1 <sub>B</sub> Fiber Mode

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
<b>Port 5 MII Interface</b>				
63	GFCEN	I	PU, LVTTTL	<p><b>Global Flow Control Enable</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(<b>RC</b>) as Flow control enable.</p> <p><i>Note: Power On Setting</i></p> <p>0<sub>B</sub> Flow Control Capability is depended upon the register setting in corresponding port's Basic Control Register</p> <p>1<sub>B</sub> All ports flow control capability is enabled</p>
	MII_P5TXD0	O	4 mA, PU, LVTTTL	<p><b>Port 5 Transmit Data Bit 0 in MII Mode</b> The LSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.</p>
	GPSI_P5TXD	O	4 mA, PU, LVTTTL	<p><b>Port 5 Transmit Data in GPSI Mode</b> When port 5 is operating in GPSI mode, this pin acts as GPSI Transmit Data. Synchronous to the rising edge of GPSI_P5TXCLK.</p>
	RMII_P5TXD0	O	4 mA, PU, LVTTTL	<p><b>Port 5 Transmit Data Bit 0 in RMII Mode</b> When port 5 is operating in RMII mode, this pin acts as RMII Transmit Data Bit[0]. Synchronous to the rising edge of REFCLK_IN.</p>
61	P5_BUSMD0	I	PD, LVTTTL	<p><b>Port 5 Bus Mode Selection Bit 0</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(<b>RC</b>) as port 5 bus mode selection bit 0. Combined with <b>P5_BUSMD1</b>, Samurai-6M/6MX (ADM6996M/MX) provides 3 bus types for port 5. P5_BUSMD[1:0], Interface</p> <p><i>Note: Power On Setting</i></p> <p>00<sub>B</sub> MII</p> <p>01<sub>B</sub> GPSI</p> <p>10<sub>B</sub> RMII</p> <p>11<sub>B</sub> Reserved and not allowed</p>
	MII_P5TXD1	O	4 mA, PD, LVTTTL	<p><b>Port 5 Transmit Data Bit 1 in MII Mode</b> The bit[1] of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.</p>
	RMII_P5TXD1	O	4 mA, PD, LVTTTL	<p><b>Port 5 Transmit Data Bit 1 in RMII Mode</b> The bit[1] of RMII Transmit data of port 5. Synchronous to the rising edge of REFCLK_IN.</p>

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
60	P5_BUSMD1	I	PD, LVTTTL	<b>Port 5 Bus Mode Selection Bit 1</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) as port 5 bus mode selection bit 1. See P5_BUSMD0 for more details. <i>Note: Power On Setting</i>
	MII_P5TXD2	O	4 mA, PD, LVTTTL	<b>Port 5 Transmit Data Bit 2 in MII Mode</b> The bit[2] of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
59	SDIO_MD	I	PD, LVTTTL	<b>SDC/SDIO Mode Selection</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) as SDC/SDIO control signal which is used to select 16 bit mode. <i>Note: Power On Setting</i> $0_B$ 16 bits mode, MDC/MDIO timing compatible
	MII_P5TXD3	O	4 mA, PD, LVTTTL	<b>Port 5 Transmit Data Bit 3 in MII Mode</b> The MSB bit of MII Transmit data of port 5. Synchronous to the rising edge of MII_P5TXCLK.
66	PHYAS0	I	PD, LVTTTL	<b>PHY Address MSB Bit 0</b> During power on reset, value will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL(RC) as PHY start address select. PHYAS[1:0] = $00_B$ and PHY address starts from $01000_B$ . <i>Note: Power On Setting</i>
	MII_P5TXEN	O	8 mA, PD, LVTTTL	<b>Port 5 Transmit Enable TXEN in MII Mode</b> Active high to indicate that the data on MII_P5TXD[3:0] is valid. Synchronous to the rising edge of MII_P5TXCLK.
	GPSI_P5TXEN	O	8 mA, PD, LVTTTL	<b>Port 5 Transmit Enable TXEN in GPSI Mode</b> Active high to indicate that the data on GPSI_P5TXD is valid. Synchronous to the rising edge of GPSI_P5TXCLK.
	RMII_P5TXEN	O	8 mA, PD, LVTTTL	<b>Port 5 Transmit Enable TXEN in RMII Mode</b> Active high to indicate that the data on RMII_P5TXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
53	MII_P5RXD0	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 0 in MII Mode</b> In MII mode, the bit is the LSB of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
	GPSI_P5RXD	I	PD, LVTTTL	<b>Port 5 Receive Data in GPSI Mode</b> In GPSI Mode, this acts as Receive Data Input, synchronous to the rising edge of GPSI_P5RXCLK.
	RMII_P5RXD0	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 0 in RMII Mode</b> In RMII mode, the bit is the LSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
54	MII_P5RXD1	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 1 in MII Mode</b> In MII mode, the bit is the bit[1] of MII receive data, synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5RXD1	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 1 in RMII Mode</b> In RMII mode, the bit is the MSB of RMII receive data, synchronous to the rising edge of REFCLK_IN.
55	MII_P5RXD2	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 2 in MII Mode</b> In MII mode, the bit is the bit[2] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
56	MII_P5RXD3	I	PD, LVTTTL	<b>Port 5 Receive Data Bit 3 in MII Mode</b> In MII mode, the bit is the bit[3] of MII receive data. Synchronous to the rising edge of MII_P5RXCLK.
52	MII_P5RXDV	I	PD, LVTTTL	<b>Port 5 Receive Data Valid in MII Mode</b> Active high to indicate that the data on MII_P5RXD[3:0] is valid. Synchronous to the rising edge of MII_P5RXCLK.
	RMII_P5CRSDV	I	PD, LVTTTL	<b>Port 5 Carrier Sense and Receive Data Valid in RMII Mode</b> Active high to indicate that the data on RMII_P5RXD[1:0] is valid. Synchronous to the rising edge of REFCLK_IN.
68	MII_P5RXER	I	PD, LVTTTL	<b>Port 5 Receive Error in MII Mode</b> Active high to indicate that there is symbol error on the MII_P5RXD[3:0]. Only valid in 100M operation.
	RMII_P5RXER	I	PD, LVTTTL	<b>Port 5 Receive Error in RMII Mode</b> Active high to indicate that there is symbol error on the RMII_P5RXD[1:0]. Only valid in 100M operation.
57	MII_P5CRS	I	PD, LVTTTL	<b>Port 5 Carrier Sense in MII Mode</b> In full duplex mode, MII_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, MII_P5CRS will be high both in receive and transmit condition.
	GPSI_P5CRS	I	PD, LVTTTL	<b>Port 5 Carrier Sense in GPSI Mode</b> In full duplex mode, GPSI_P5CRS reflects the receive carrier sense situation on medium only; In Half Duplex, GPSI_P5CRS will be high both in receive and transmit condition.
58	MII_P5COL	I	PD, LVTTTL	<b>Port 5 Collision Input in MII Mode</b> Active high to indicate that there is collision on the medium. Stay low in full duplex operation.
	GPSI_P5COL	I	PD, LVTTTL	<b>Port 5 Collision Input in GPSI Mode</b> Active high to indicate that there is collision on the medium. Stay low in full duplex operation.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
72	MII_P5RXCLK	I	PD, LVTTTL	<b>Port 5 Receive Clock Input in MII Mode</b> MII_P5RXDV and MII_P5RXD[3:0] are synchronous to the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode.
	GPSI_P5RXCLK	I	PD, LVTTTL	<b>Port 5 Receive Clock Input in GPSI Mode</b> GPSI_P5RXD are synchronous to the rising edge of this clock. It is non-continuous 10 MHz Clock input.
	REFCLK_IN	I	PD, LVTTTL	<b>50MHz Reference Clock Input in RMII Mode</b> RMII_P5RXD[1:0], RMII_P5TXD[1:0], RMII_P5TXEN and RMII_P5CRSDV are synchronous to the rising edge of this clock.
67	MII_P5TXCLK	I	PD, LVTTTL	<b>Port 5 Transmit Clock Input in MII Mode</b> MII_P5TXEN and MII_P5TXD[3:0] are output at the rising edge of this clock. It is free running 25 MHz clock in 100M mode and 2.5 MHz clock in 10M mode.
	GPSI_P5TXCLK	I	PD, LVTTTL	<b>Port 5 Transmit Clock Input in GPSI Mode</b> GPSI_P5TXEN and GPSI_P5TXD are synchronous to the rising edge of this clock. It is continuous 10 MHz Clock input.
	REFCLK_OUT	O	8 mA, PD, LVTTTL	<b>50MHz Reference Clock Output in RMII Mode</b> This pin is used as 50 MHz reference clock signal output pin when port 5 operates in RMII mode.
89	SPDTNP5	I	PD, LVTTTL	<b>Port 5 Speed Input</b> This pin is used to select the speed mode of Port 5. 0 <sub>B</sub> 100M 1 <sub>B</sub> 10M
90	LNKFP5	I	PD, LVTTTL	<b>Port 5 Link Fail Status Input</b> This pin is used as link control of Port 5. 0 <sub>B</sub> Link Up 1 <sub>B</sub> Link Failed
91	DPHALFP5	I	PD, LVTTTL	<b>Port 5 Duplex Status Input</b> This pin is used to select the duplex mode of Port 5. 0 <sub>B</sub> Full Duplex 1 <sub>B</sub> Half Duplex

**LED Interface**

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
107	DPHALFP4	I	PD, LVTTTL	<b>Port 4 Duplex status Input</b> When Port 4 operates under MAC MII mode (see <b>CFG0</b> for more details), this pins is used to select the duplex mode of Port 4. $0_B$ Full Duplex $1_B$ Half Duplex
	DUPCOL4	O	8 mA, PD, LVTTTL	<b>Port 4 Duplex /Collision LED</b> When Port 4 operates under PHY or PCS MII mode (see <b>CFG0</b> for more details), in Full duplex mode, this pin acts as DUPLEX LED for Port 4; in half duplex mode, it is collision LED for each port. See <b>Chapter 3.1.12 LED Display</b> for more details.
110	DUPCOL3	O	8 mA, PD, LVTTTL	<b>Port 3 Duplex /Collision LED</b> In Full duplex mode, this pin acts as DUPLEX LED for Port 3; in half duplex mode, it is collision LED for each port. See <b>Chapter 3.1.12 LED Display</b> for more details.
111	BPEN	I	PU, LVTTTL	<b>Recommend Back-Pressure in Half-Duplex</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) during power on reset as the back-pressure enable in half-duplex mode. <i>Note: Power On Setting</i> $0_B$ Disable Back-Pressure $1_B$ Enable Back-Pressure
	DUPCOL2	O	8 mA, PU, LVTTTL	<b>Port 2 Duplex-collision LED</b> In Full duplex mode, this pin acts as Port 2 DUPLEX LED; in half duplex mode, it is collision LED for Port 2. See <b>Chapter 3.1.12 LED Display</b> for more details.
112	PHYAS1	I	PD, LVTTTL	<b>Recommend PHY Address Bit 1</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) during power on reset as the PHY address recommends value bit 1. See <b>PHYAS0</b> description for more details. <i>Note: Power On Setting</i>
	DUPCOL1	O	8 mA, PD, LVTTTL	<b>Port 1 Duplex-collision LED</b> In Full duplex mode, this pin acts as port 1 DUPLEX LED; in half duplex mode, it is collision LED for Port 1. See <b>Chapter 3.1.12 LED Display</b> for more details.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
113	RECANEN	I	PU, LVTTTL	<b>Recommend Auto Negotiation Enable</b> Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. <i>Note: Power On Setting.</i> 0 <sub>B</sub> Disable all TP port auto negotiation capability 1 <sub>B</sub> Enable all TP port auto negotiation capability
	DUPCOL0	O	8 mA, PU, LVTTTL	<b>Port 0 Duplex-collision LED</b> In Full duplex mode, this pin acts as port 0 DUPLEX LED; in half duplex mode, it is collision LED for Port 0. See <a href="#">Chapter 3.1.12 LED Display</a> for more details.
92	LNKFP4	I	PD, LVTTTL	<b>Port 4 Link Fail Status Input</b> When Port 4 operates under MAC MII mode (see <a href="#">CFG0</a> for more details), this pin is used as link control of Port 4. 0 <sub>B</sub> Link Up 1 <sub>B</sub> Link Failed
	LNKACT_4	O	8 mA, PD, LVTTTL	<b>LINK/Activity LED of Port 4</b> When Port 4 operates under PHY or PCS MII mode (see <a href="#">CFG0</a> for more details), this pin is used to indicate the link/activity status of Port 4, see <a href="#">Chapter 3.1.12 LED Display</a> for more details.
95	LNKACT_3	O	8 mA, PD, LVTTTL	<b>LINK/Activity LED of Port 3 to 0</b> Used to indicate corresponding port' s link/activity status, see <a href="#">Chapter 3.1.12 LED Display</a> for more details.
96	LNKACT_2			
97	LNKACT_1			
98	LNKACT_0			
51	SPDTNP4	I	PD, LVTTTL	<b>Port 4 Speed Input</b> When Port 4 operates under MAC MII mode (see <a href="#">CFG0</a> for more details), this pin is used to select the operating speed of Port 4. 0 <sub>B</sub> 100M 1 <sub>B</sub> 10M
	LDSPD_4	O	8 mA, PD, LVTTTL	<b>Port 4 Speed LED</b> When Port 4 operates under PHY or PCS MII mode (see <a href="#">CFG0</a> for more details), this pin is used to indicate the speed status of Port 4, see <a href="#">Chapter 3.1.12 LED Display</a> for more details.
48	LDSPD_3	O	8 mA, PD, LVTTTL	<b>Port 3 to Port 0 Speed LED</b> Used to indicate corresponding port' s speed status, see <a href="#">Chapter 3.1.12 LED Display</a> for more details.
47	LDSPD_2			
43	LDSPD_1			
42	LDSPD_0			

**EEPROM Interface**



**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
84	EDO	I	PU, LVTTTL	<b>EEPROM Data Output</b> This pin is used to input EEPROM data when reading EEPROM. During Samurai-6M/6MX (ADM6996M/MX) initialisation, Samurai-6M/6MX (ADM6996M/MX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See <a href="#">Chapter 3.4.2 EEPROM Interface</a> for more details.
80	IFSEL	I	PD, LVTTTL	<b>Interface Selection</b> After Samurai-6M/6MX (ADM6996M/MX) initialization process is done, this pin is used to select using EEPROM interface or SDC/SDIO interface. EECS/IFSEL interface 0 <sub>B</sub> SDC/SDIO interface 1 <sub>B</sub> EEPROM interface
	EECS	O	4 mA, PD, LVTTTL	<b>EEPROM Chip Select</b> During Samurai-6M/6MX (ADM6996M/MX) initialisation, this pin is used as EEPROM chip select signal. During Samurai-6M/6MX (ADM6996M/MX) initialize itself, Samurai-6M/6MX (ADM6996M/MX) will drive EEPROM interface signal to read settings from EEPROM. Any other devices attached to EEPROM interface SHOULD drive Hi-Z or keep tristate during this period. See <a href="#">Chapter 3.4.2 EEPROM Interface</a> for more details.
81	XOVEN	I	PD, LVTTTL	<b>Cross Over Enable</b> Value on this pin (active low) will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL( <b>RC</b> ) for Port 4~0 crossover auto detect (Only available in TP interface). <i>Note: Power On Setting.</i> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
	EESK	I/O	4 mA, PD, LVTTTL	<b>EEPROM Serial Clock</b> During Samurai-6M/6MX (ADM6996M/MX) initialisation, this pin is used to output clock to EEPROM. After Samurai-6M/6MX (ADM6996M/MX) initialization process is done, this pin is used as EEPROM interface clock input if <b>IFSEL</b> = 1.
	SDC	I	PD, LVTTTL	<b>Serial Management interface Clock input</b> If <b>IFSEL</b> = 0, this pin is used as serial management interface clock input.

**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
79	LED_MODE	I	PD, LVTTTL	<b>Enable Mac to Choose LED Display Mode</b> Value on this pin will be latched by Samurai-6M/6MX (ADM6996M/MX) at the rising edge of RESETL( <b>RC</b> ) as single/dual color LED mode control signal. See <a href="#">Chapter 3.1.12 LED Display</a> for more details. <i>Note: Power On Setting.</i>
	EDI	I/O	8 mA, PD, LVTTTL	<b>EEPROM Serial Data Input</b> During Samurai-6M/6MX (ADM6996M/MX) initialize itself, this pin is used to output address and command to access EEPROM. After the initialization process is done, this pin becomes an input pin to monitor EEPROM data if <b>IFSEL</b> = 1.
	SDIO	I/O	8 mA, PD, LVTTTL	<b>Serial Management interface Data input/Output</b> If <b>IFSEL</b> = 0, this pin is used as data input/output pin of serial management interface.

**Power/Ground, 48 Pins**

4, 5, 12, 13, 20, 27, 28, 34, 35	GNDA	GND	–	<b>Ground</b> Used by AD Block
1, 9, 17, 24, 38	VCCA2	PWR	–	<b>1.8 V, Power</b> Used by TX Line Driver
8, 16, 23, 31	VCCAD	PWR	–	<b>3.3 V, Power</b> Used by AD Block
126	GNDBIAS	GND	–	<b>Ground</b> Used by Bias Block
128	VCCBIAS	PWR	–	<b>3.3 V, Power</b> Used by Bias Block.
123	GNDPLL	GND	–	<b>Ground</b> Used by PLL
122	VCCPLL	PWR	–	<b>1.8 V, Power</b> Used by PLL
45, 64, 76, 83, 93, 118	GNDIK	GND	–	<b>Ground</b> Used by Digital Core
46, 75, 82, 94, 116	VCCIK	PWR	–	<b>1.8 V, Power</b> Used by Digital Core
50, 70, 87, 99, 108	GND0	GND	–	<b>Ground</b> Used by Digital Pad
49, 71, 88, 109	VCC30	PWR	–	<b>3.3 V, Power</b> Used by Digital Pad

**Miscellaneous**

41	TEST	I	PD, LVTTTL	<b>Test Mode</b> Reserved and should keep 0 when normal operation.
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**Table 3 IO Signals (cont'd)**

Ball No.	Name	Pin Type	Buffer Type	Function
86	CFG0	I	PU, LVTTTL	<b>Configuration 0</b> Combined with <b>P4_BUSMD0</b> and <b>P4_BUSMD1</b> , Samurai-6M/6MX (ADM6996M/MX) provides 3 bus type for port 4. {CFG0, P4_BUSMD[1:0]}, Bus Mode of Port 4 0_00 <sub>B</sub> PHY Interface 0_01 <sub>B</sub> MAC MII 1_XX <sub>B</sub> PCS MII
69	WAIT_INIT	I	PD, LVTTTL	<b>Wait Initialization</b> This pin will be used to pause all activities after power up until EEPROM is loaded successfully or CPU initialization is done.. 0 <sub>B</sub> pause until loading EEPROM is done. 1 <sub>B</sub> pause until EEPROM successfully loaded or CPU initialization is done.
65	INT_N	O	OD,8 mA	<b>Interrupt</b> Active low interrupt signal to indicate the status change in the interrupt status register. Interrupt signal will keep active low until host read the status of ISR register. 0 <sub>B</sub> Interrupt 1 <sub>B</sub> Not interrupt
40	MDIO	I/O	8 mA, PD, LVTTTL	<b>Management Data</b> MDIO transfers management data in and out of the device synchronous to MDC.
44	MDC	I	PD, ST	<b>Management Data Reference Clock</b> A non-continuous clock input for management usage. Samurai-6M/6MX (ADM6996M/MX) will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
85	CKO25M	O	8 mA, PD, LVTTTL	<b>25M Clock Output</b> Free Running 25M Clock output (Even during power on reset)
119	RC	I	ST	<b>RC Input For Power On Reset</b> This pin is sampled by using the 25 MHz free running clock signal which gets the input from <b>XI</b> to generate the low-active reset signal, RESETL. See <b>Chapter 5.3.2 Power On Reset</b> for the timing requirements.
120	XI	AI	ANA	<b>25MHz Crystal /Oscillator Input</b> 25MHz Crystal or Oscillator Input. Variation is limited to +/- 50ppm.
121	XO	AO	ANA	<b>25MHz Crystal Output</b> When connected to oscillator, this pin should be left unconnected.
127	RTX	AI	ANA	<b>Constant Voltage Reference</b> External 1.0 kΩ 1% resistor connection to ground.

**Table 3 IO Signals (cont'd)**

<b>Ball No.</b>	<b>Name</b>	<b>Pin Type</b>	<b>Buffer Type</b>	<b>Function</b>
125	VREF	AI	ANA	<b>Analog Reference Voltage</b> Used by Internal Bias Circuit for voltage reference. External 0.1uF capacitor connection to ground for noise filter.
124	CONTROL	AI/O	ANA	<b>FET Control Signal</b> The pin is used to control FET for 3.3 V to 1.8 V regulator. External 0.1uF capacitor connection to ground for noise filter, even the pin is un-connected.

## 3 Function Description

### 3.1 Switch Functional Description

The Samurai-6M/6MX (ADM6996M/MX) uses the “store & forward” switching approach for the following reasons:

1. Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require large elastic buffers, especially when bridging between a server on a 100 Mbit/s network and clients on a 10 Mbit/s segment
2. Store & forward switches improve overall network performance by acting as a “network cache”
3. Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port

#### 3.1.1 Basic Operation

The Samurai-6M/6MX (ADM6996M/MX) receives incoming packets from one of its ports, uses the source address (SA) and FID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and FID.

If the DA and FID are not found in the address table, the Samurai-6M/6MX (ADM6996M/MX) treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.

The Samurai-6M/6MX (ADM6996M/MX) can automatically learn the port number of attached network devices together with the SA and FID of all the incoming packets. If the SA and FID are not found in the address table, the Samurai-6M/6MX (ADM6996M/MX) adds it to the table.

#### 3.1.2 Buffers and Queues

The Samurai-6M/6MX (ADM6996M/MX) incorporates 6 transmit queues and receive buffer areas for the 6 Ethernet ports. The receive buffers, as well as the transmit queues, are located within the Samurai-6M/6MX (ADM6996M/MX) along with the switch fabric. The buffers are divided into 192 blocks of 256 bytes each. The queues of each port are managed according to each port’s read/write pointer.

Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

#### 3.1.3 Full Duplex Flow Control

When a full duplex port runs out of its receive buffers, a PAUSE command will be issued by Samurai-6M/6MX (ADM6996M/MX) to notify the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When the flow control hardware pin (**GFCEN**) is set to high, during power on reset, and per port PAUSE is enabled, Samurai-6M/6MX (ADM6996M/MX) will output and accept 802.3x flow control packets.

#### 3.1.4 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation. When the Samurai-6M/6MX (ADM6996M/MX) cannot allocate a receive buffer for the incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

#### 3.1.5 Back-Off Algorithm

The Samurai-6M/6MX (ADM6996M/MX) implements the truncated exponential back off algorithm compliant to the 802.3 standard. Samurai-6M/6MX (ADM6996M/MX) will restart the back off algorithm by choosing 0-9 collision

count. After 16 consecutive retransmit trials, the Samurai-6M/6MX (ADM6996M/MX) resets the collision counter. Users can set the Back Off (see 0010<sub>H</sub>, **BD**) to disable this function.

### 3.1.6 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6 μs for 10 Mbit/s Ethernet and 960 ns for 100 Mbit/s fast Ethernet. For the receive end, Samurai-6M/6MX (ADM6996M/MX) is designed to tolerate IPG gaps greater than 64 bits. For the transmit end, Samurai-6M/6MX (ADM6996M/MX) will always transmit packets with the minimum IPG gap equal to 96 bits. If users want to shorten the transmission IPG gap, users can enable the Short IPG function (see 000B<sub>H</sub>, **TSIE**). Then Samurai-6M/6MX (ADM6996M/MX) will instruct its output MAC to transmit packets in average 92 bits IPG gap.

### 3.1.7 Trunking Function

Samurai-6M/6MX (ADM6996M/MX) supports only one trunking port. If Port 3 and Port 4 Trunk (see 000B<sub>H</sub>, **TE**) function is enabled, Samurai-6M/6MX (ADM6996M/MX) will treat Port 3 and Port 4 as the same port to make the bandwidth equal to 200M. When any of these two ports link fail, the Samurai-6M/6MX (ADM6996M/MX) will automatically change the transmit path from the failed link port to linked one. Output port based load balancing is implemented in Samurai-6M/6MX (ADM6996M/MX), without any users' setting.

### 3.1.8 Illegal Frames

The Samurai-6M/6MX (ADM6996M/MX) will discard all illegal packets. These packets are

1. Undersized packets: The packets received with the length of less than 64 bytes are discarded
2. Oversized packets: The packets received with the length of more than "MAXPKTLEN" bytes are discarded. See (0011<sub>H</sub>, **MPL**) to see how to set the MAXPKTLEN value
3. CRC packets: The packets received with a wrong FCS value are discarded
4. Symbol error packets: The packets received with symbol error are discarded
5. Source violation packets: The packets received with a source violation could be discarded in some cases. See (**Source Violation**) description.
6. VLAN violation packets: The frames received with a VLAN violation can be discarded in some cases. See (**VLAN Violation**) description

### 3.1.9 Broadcast Storm

Samurai-6M/6MX (ADM6996M/MX) allows users to limit the traffic of the broadcast address (DA = FFFFFFFF<sub>H</sub>) to prevent them from blocking the switch bandwidth. If users also want to limit the multicast packets (DA[40] = 1<sub>B</sub>), they can set the Multicast Packet Counted into Storming Counter (see 0010<sub>H</sub>, **MP**) function. Two threshold and storm enable bits (see 003B<sub>H</sub> and 003C<sub>H</sub>, **STORM\_EN**, **STORM\_100\_TH**, **STORM\_10\_TH**) are used to control the broadcast storm.

1. Time Scale. Samurai-6M/6MX (ADM6996M/MX) uses 50ms on a scale to meter the storm packets.

Parameter	Rising Threshold	Falling Threshold
All link ports are 100M	100M Threshold (See 003B <sub>H</sub> )	1/2 100M Threshold
Not All link ports are 100M	10M Threshold (See 003C <sub>H</sub> )	1/2 10M Threshold

2. Storm keeps on at least 1.6 seconds if any of the ports meet the rising threshold in the 4 consecutive 50 ms intervals. In these 1.6 seconds, the ports meet the rising threshold and will start to discard the broadcast or multicast packets until the 50 ms interval expires. Users could also disable Input Filter (see 000B<sub>H</sub>, **IF**) function to forward above packets to the un-congested port instead of discarding directly.

3. Storm finishes. After the 1.6-second storm period, Samurai-6M/6MX (ADM6996M/MX) will check the port that makes the storm on. If all of these ports meet the falling threshold in the 2 consecutive 50 ms intervals and no

other ports meet the rising threshold at the same time, Samurai-6M/6MX (ADM6996M/MX) will treat it the storm has finished.

### 3.1.10 Bandwidth Control

Samurai-6M/6MX (ADM6996M/MX) supports hardware-based bandwidth control for both ingress and egress traffic. Ingress and egress rate can be limited independently on each port base. The Samurai-6M/6MX (ADM6996M/MX) provides several timer scales corresponding to different the bandwidth control unit, so users can configure the rate equal to  $K * (\text{Bandwidth Step})$ ,  $1 \leq K \leq 2048$ . Different timer scales can optimize the QoS performance by different bandwidth control unit. Samurai-6M/6MX (ADM6996M/MX) maintains two counters (input and output) for each port. For example, if users want to limit rate equal to 64 kbit/s, they should configure the bandwidth control threshold equal to 1. At each time unit, Samurai-6M/6MX (ADM6996M/MX) will add 64 to the counter and decrease the byte length when receiving a packet in this period. When the counter is decreased to zero, we can divide the control behavior into two parts:

For the ingress control, the ingress port will not receive packets any more. If flow control is enabled, Pause packets will be transmitted, if Back Pressure is enabled, Jam packets will be transmitted, and if the above functions are not enabled, the packets will be discarded.

For the egress control, the egress port will not transmit any packets, so the egress bandwidth is controlled.

Samurai-6M/6MX (ADM6996M/MX) allows users to control the ingress and egress bandwidth at the same time (see 0033<sub>H</sub>, [Bandwidth Control Enable Register](#)).

For Example, set P0 receive bandwidth control to 6 Mbit/s.

1. Set the receive bandwidth of P0.  $N = \{R0BW\_TH3, R0BW\_TH2, R0BW\_TH1, R0BW\_TH0, 6'b0\} = 0x005e$
2. Enable P0 receive bandwidth control. Set 0033<sub>H</sub>[0]=1

**Table 4 Bandwidth Control Timer Select**

0029 <sub>H</sub> [10:9]	Timer Scale	Bandwidth Step	Applied Range
00	8ms	64Kbps	64Kbps~2.2Mbps
01	1ms	512Kbps	512Kbps~18Mbps
10	40us	200Kbps	200Kbps~100Mbps
11	500us	16Kbps	16Kbps~32Mbps

### 3.1.11 Smart Discard

The Samurai-6M/6MX (ADM6996M/MX) supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

**Table 5 Smart Disacrd**

Queue	Discard Mode
Queue 3	Discard Mode of Queue 3 in 0010 <sub>H</sub> [15:14]
Queue 2	Discard Mode of Queue 2 in 0010 <sub>H</sub> [13:12]
Queue 1	Discard Mode of Queue 1 in 0010 <sub>H</sub> [11:10]
Queue 0	Discard Mode of Queue 0 in 0010 <sub>H</sub> [9:8]

**Table 6 Discard Ratio**

Discard Mode	00	01	10	11
Utilization 00	0%	0%	0%	0%

**Table 6 Discard Ratio (cont'd)**

Discard Mode	00	01	10	11
Utilization 01	0%	0%	25%	50%
Utilization 11	0%	25%	50%	75%

### 3.1.12 LED Display

Three LEDs per port are provided by Samurai-6M/6MX (ADM6996M/MX): Link/Act, Duplex/Col and Speed. The dual-color LED mode is also supported by Samurai-6M/6MX (ADM6996M/MX). For easy production purpose, the test signal is sent to each LED at power on reset stage. The LED display mode is controlled by:

1. **DUAL-COLOR-EE** (see 0012<sub>H</sub>): It is an EEPROM register to control the dual or single color mode. It is useless when the value (wait\_init) on the pin **WAIT\_INIT** is low.
2. **LED\_MODE**: It is the value latched on the EDI pin during the power on reset. It's also used to control the dual or single color mode and is useless when the value (wait\_init) is high.
3. **LED-ENABLE** (see 0012<sub>H</sub>): When CPU is attached and this CPU has no ability to pull the EDI to high or low, users may set the wait\_init to high to delay the led test, write the correct value to the **DUAL-COLOR-EE**, write 1<sub>B</sub> into register **LED-ENABLE**, and then the LED test starts.
4. **DUP\_COL\_SEP** (see 0012<sub>H</sub>): Dupcol LEDs indicate the duplex status only.
5. **DHCOL\_LED\_EN** (See 0030<sub>H</sub>): When enabled, pin DUPCOL0 shows col\_10m status and pin DUPCOL1 shows col\_100m status. These two LEDs are necessary in the dual-speed hub.

#### 3.1.12.1 Single Color LED Display

**Table 7 Single Color LED Display**

Pin Name	Status
LNKACT4/LNKACT3/ LNKACT2/LNKACT1/ LNKACT0	<p>These pins have no power on reset values on them, and Samurai-6M/6MX (ADM6996M) uses active low value to drive the LED. So the output values of these pins after the power on reset are shown as follows:</p> <ol style="list-style-type: none"> <li>1. First period: This period lasts 1.28 s for LED on test. Samurai-6M/6MX (ADM6996M/MX) drives value 0 to open the LED.</li> <li>2. Second period: This period lasts 0.48 s for LED off test. Samurai-6M/6MX (ADM6996M/MX) drives value 1 to close the LED.</li> <li>3. Normal Period: This period indicates the link status.</li> </ol> <p>0<sub>B</sub> Port links up and LED is ON. 1<sub>B</sub> Port links down and LED is OFF. 0/1<sub>B</sub> Port links up and is transmitting or receiving. The LED flashes at 10 Hz.</p>
LDSPD4/LDSPD3/ LDSPD2/LDSPD1/ LDSPD0	<p>The behavior of these pins is the same as the LNKACT, except for the normal period.</p> <p>Normal period: This period indicates the speed status.</p> <p>0<sub>B</sub> Port links up and its speed is 100M. LED is ON. 1<sub>B</sub> Port links down or its speed is 10M. LED is OFF.</p>



**Table 7 Single Color LED Display (cont'd)**

Pin Name	Status
DUPCOL2/ DUPCOL1/ DUPCOL0	<p>These 3 pins have power on reset values on them. Samurai-6M/6MX (ADM6996M/MX) needs to consider these values to drive the correct value. If the power on reset value is value_power_on, then the display is as follows:</p> <ol style="list-style-type: none"> <li>1. First period: This period lasts 1.28 s for LED on test. Samurai-6M/6MX (ADM6996M/MX) drives ~value_power_on to open the LED.</li> <li>2. Second period: This period lasts 0.48 s for LED off test. Samurai-6M/6MX (ADM6996M/MX) drives value_power_on to close the LED.</li> <li>3. Normal Period: This period indicates the duplex/collision status. <ul style="list-style-type: none"> <li>~value_power_on = Port links up in the full-duplex mode. LED is ON.</li> <li>value_power_on = Port links down. LED flashes at 10 Hz.</li> <li>0/1<sub>B</sub> Port links up and collision is detected. The LED flashes at 10 Hz.</li> </ul> </li> </ol> <p>If <b>DUP_COL_SEP</b> is enabled, the normal period changes its way to display.</p> <ul style="list-style-type: none"> <li>~value_power_on = Port links up in the duplex mode. LED is ON.</li> <li>value_power_on = Port links down or links up in the half-duplex mode. LED is OFF.</li> <li>0/1<sub>B</sub> This value is cancelled. LED doesn't blink.</li> </ul> <p>If <b>DHCOL_LED_EN</b> is enabled, the display in the normal period is as follows:</p> <p>DUPCOL0: 10m collision indicator.</p> <ul style="list-style-type: none"> <li>0/1<sub>B</sub> One of the ports links up in 10M half-duplex mode and detects a collision event. The LED flashes at 20 Hz.</li> <li>value_power_on = When the above event is not satisfied, the LED is OFF.</li> </ul> <p>DUPCOL1: 100 m collision indicator.</p> <ul style="list-style-type: none"> <li>0/1<sub>B</sub> One of the ports links up in 100M half-duplex mode and detects a collision event. The LED flashes at 20 Hz.</li> <li>value_power_on = The above event is not satisfied. LED is OFF.</li> </ul>
DUPCOL4/ DUPCOL3	<p>The behavior of these pins is the same as the LNKACT, except the normal period.</p> <p>Normal period: This period indicates the duplex/collision status.</p> <ul style="list-style-type: none"> <li>~value_power_on = Port links up in the full-duplex mode. LED is ON.</li> <li>value_power_on = Port links down. LED is OFF.</li> <li>0/1<sub>B</sub> Port links up and collision is detected. The LED flashes at 10 Hz.</li> </ul> <p>If <b>DUP_COL_SEP</b> is enabled, the normal period changes its way to display.</p> <ul style="list-style-type: none"> <li>~value_power_on = Port links up in the duplex mode. LED is ON.</li> <li>value_power_on = Port links down or links up in the half-duplex mode. LED is OFF.</li> <li>0/1<sub>B</sub> This value is cancelled. LED doesn't blink.</li> </ul>

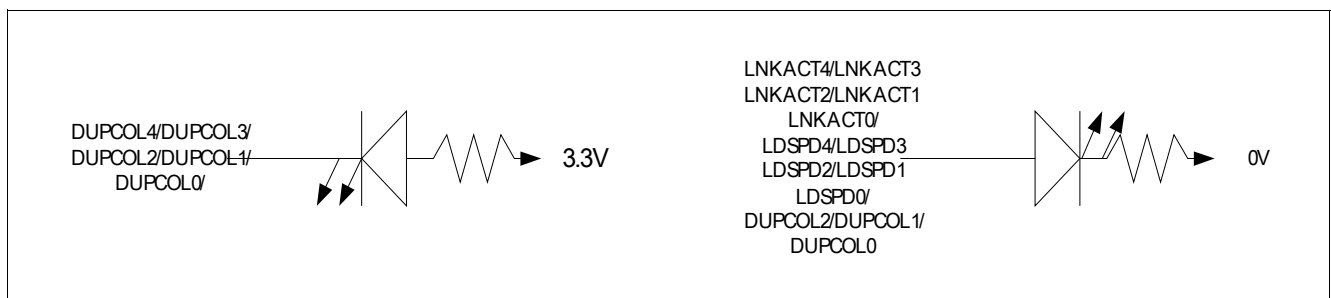
### 3.1.12.2 Dual Color LED Display

Users should be careful that DUPCOL LED only supports the single color mode. The only difference between single and dual color for DUPCOL LED is the self-test time.

**Table 8 Dual Color LED Display**

Pin Name	Status
(LNKACT4, LDSPD4)/ (LNKACT3, LDSPD3) (LNKACT2, LDSPD2) (LNKACT1, LDSPD1) (LNKACT0, LDSPD0)	<p>First Period: Test LED on with green color. It lasts 1.28 s. 01<sub>B</sub> LED is on with green color.</p> <p>Second Period: Test LED on with yellow color. It lasts 1.28 s. 10<sub>B</sub> LED is on with yellow color.</p> <p>Third period: Test LED off. 00<sub>B</sub> LED is off.</p> <p>Normal Period: This period shows the status of the link and speed at the same time.</p> <p>00<sub>B</sub> Port links down. LED is off. 11<sub>B</sub> Port links down. LED is off. 01<sub>B</sub> Port links up in 100M. LED glows green. 10<sub>B</sub> Port links up in 10M. LED glows yellow. 0/1,1<sub>B</sub> Port links up in 100M and is receiving or transmitting. LED blinks with green color at 10 Hz. 0/1,0<sub>B</sub> Port links up in 10M and is receiving or transmitting. LED blinks with yellow color at 10 Hz.</p>
DUPCOL4/DUPCOL3/ DUPCOL2/DUPCOL1/ DUPCOL0	The behavior of these pins is the same as the single mode, except the self-test period. The LED on test period is 2.56 s instead of 1.28 s.

### 3.1.12.3 Circuit for Single LED Mode



**Figure 3 Circuit for Single Color LED Mode**

### 3.1.12.4 Circuit for Dual LED Mode

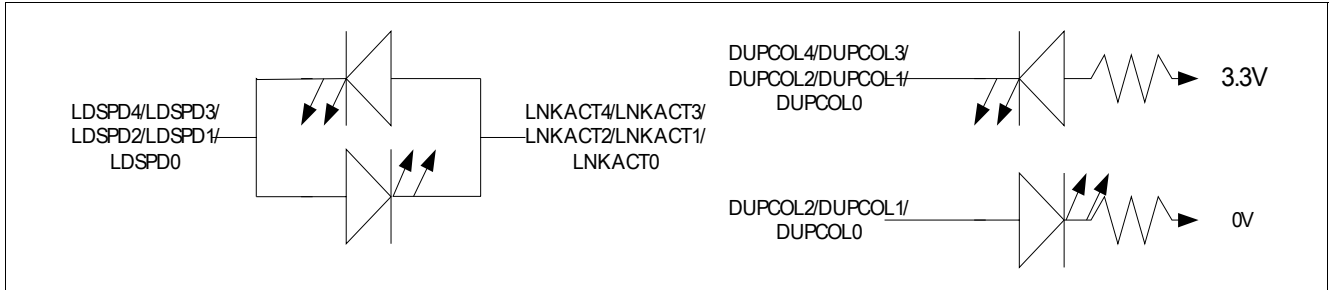


Figure 4 Circuit for Dual Color LED Mode

### 3.1.13 Packet Identification

Packets are classified to determine if they should be passed to the CPU port or another entity for special handling.

Table 9 Packet Identification

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)	Comments
BPDU	The Ethernet destination address is 01 80 C2 00 00 00 <sub>H</sub> .
PAUSE	The Ethernet destination address is 01 80 C2 00 00 01 <sub>H</sub> . Ether-Type field is 8808 <sub>H</sub> . OPCODE is 0001 <sub>H</sub> .
SLOW	The Ethernet destination address is 01 80 C2 00 00 02 <sub>H</sub> .
PAE	The Ethernet destination address is 01 80 C2 00 00 03 <sub>H</sub> .
RESER_R0	The Ethernet destination address ranges between 01 80 C2 00 00 04 <sub>H</sub> and 01 80 C2 00 00 0F <sub>H</sub> .
RESER_R1	The Ethernet destination address ranges between 01 80 C2 00 00 10 <sub>H</sub> and 01 80 C2 00 00 1F <sub>H</sub> .
GXRP	The Ethernet destination address ranges between 01 80 C2 00 00 20 <sub>H</sub> and 01 80 C2 00 00 22 <sub>H</sub> .
RESER_R2	The Ethernet destination address ranges between 01 80 C2 00 00 23 <sub>H</sub> and 01 80 C2 00 00 2F <sub>H</sub> .
RESER_R3	The Ethernet destination address ranges between 01 80 C2 00 00 30 <sub>H</sub> and 01 80 C2 00 00 FF <sub>H</sub> .
RARP	The Ethernet destination address is FF FF FF FF FF FF <sub>H</sub> and the Ether-Type field is 8035 <sub>H</sub> .
ARP	The Ethernet destination address is FF FF FF FF FF FF <sub>H</sub> and the Ether-Type field is 8036 <sub>H</sub> .
IGMP_IP	The Ethernet destination address is 01 00 5E xx xx xx <sub>H</sub> . Ether-Type field is 0800 <sub>H</sub> (IP). IP Version is 4 and the Protocol field is 02 <sub>H</sub> (IGMP).
MLD_IP	Ethernet destination address is 33 33 xx xx xx xx <sub>H</sub> . The Ether-Type field is 0800 <sub>H</sub> (IP). IP Version is 6 and the Protocol field is 3A <sub>H</sub> (ICMP).
MLD_IPV6	Ethernet destination address is 33 33 xx xx xx xx <sub>H</sub> . The Ether-Type field is 86DD <sub>H</sub> (IP). IP Version is 6 and the Protocol field is 3A <sub>H</sub> (ICMP).

**Table 9 Packet Identification** (cont'd)

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)		Comments
Others	TYPE	The Ether-Type field matches one of the type filters.
	PROTOCOL	The Protocol field matches one of the protocol filters.
	TCPUDP	The TCP/UDP port number matches one of the TCP/UDP filters.
	MAC_CTRL	The Ether-Type field is 8808 <sub>H</sub> , but OPCODE is not 0001 <sub>H</sub> .

For learning purpose, Samurai-6M/6MX (ADM6996M/MX) sometimes divides Ethernet address into three groups.

**Table 10 Packet Identification Groups**

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)	Comments
MULTICAST	The first bit of the Ethernet destination address is 1, but not all 1.
BROADCAST	The Ethernet destination address is FF FF FF FF FF FF <sub>H</sub> .
UNICAST	The first bit of the Ethernet destination address is 0.

### 3.1.13.1 Span Packet

Samurai-6M/6MX (ADM6996M/MX) supports 4 Spanning Tree Port State (Disable, Blocking/Listening, Learning and Forwarding state) for every port to enable Spanning Tree Protocol function when co-operates with an external CPU. These port states are defined in **STPS** of EEPROM register 0013<sub>H</sub> ~ 0018<sub>H</sub>.

Samurai-6M/6MX (ADM6996M/MX) supports a function to specify a packet to be treated as a Span Packet. Beside Disable state, the Span Packets will not be dropped by Spanning Tree Port State settings.

**Table 11 Span Packet**

Packet Type	Description
<b>BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3</b>	The span packet is determined in priority order by: <ol style="list-style-type: none"> <li>Span bit defined in the Special TAG, when Span_Valid is set.</li> <li>Span bit defined in the learning table when there is a match for DA+FID.</li> <li>Span bit defined in the control table when there is a match for DA.</li> <li>Span bit in register 003E<sub>H</sub>.</li> </ol>
<b>ARP/RARP</b>	The span packet is determined in priority order by: <ol style="list-style-type: none"> <li>Span bit defined in the Special TAG, when Span_Valid is set.</li> <li>Span bit in register 000D<sub>H</sub>.</li> </ol>
<b>IGMP_IP/MLD_IP/MLD_IPV6</b>	The span packet is determined in priority order by: <ol style="list-style-type: none"> <li>Span bit defined in the Special TAG, when Span_Valid is set.</li> <li>Span bit in register 000C<sub>H</sub>.</li> </ol>
<b>Others</b>	The span packet is determined in priority order by: <ol style="list-style-type: none"> <li>Span bit defined in the Special TAG, when Span_Valid is set.</li> <li>Span bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-span packets.</li> </ol>

### 3.1.13.2 Management Packet

Samurai-6M/6MX (ADM6996M/MX) reserves some buffers for these packets, so they are not dropped because of traffic congestion. Management packets are never limited by the bandwidth control, stormed by the storming control, or dropped due to **Smart Discard** function.

**Table 12 Management Packet**

Packet Type	Description
<b>BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3</b>	The management packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Management bit defined in the Special TAG, when Management_Valid is set.</li> <li>2. Management bit defined in the learning table when there is a match for DA+FID.</li> <li>3. Management bit defined in the control table when there is a match for DA.</li> <li>4. Management bit in register 003E<sub>H</sub>.</li> </ol>
<b>ARP/RARP</b>	The management packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Management bit defined in the Special TAG, when Management_Valid is set.</li> <li>2. Management bit in register 000D<sub>H</sub>.</li> </ol>
<b>IGMP_IP/MLD_IP/MLD_IPV6</b>	The management packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Management bit defined in the Special TAG, when Management_Valid is set.</li> <li>2. Management bit in register 000C<sub>H</sub>.</li> </ol>
<b>Others</b>	The management packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Management bit defined in the Special TAG, when Management_Valid is set.</li> <li>2. Management bit defined in the learning table when there is a match for DA+FID. If the first and second conditions are not satisfied, the frame is classified as non-management packets.</li> </ol>

### 3.1.13.3 Cross\_VLAN Packet

Cross-VLAN packets are defined to cross VLAN boundary or bypass the VLAN violation.

**Table 13 Cross\_VLAN Packet**

Packet Type	Description
<b>BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3</b>	The cross-VLAN packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Cross_VALN bit defined in the Special TAG, when Cross_VLAN_Valid is set.</li> <li>2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID.</li> <li>3. Cross_VLAN bit defined in the control table when there is a match for DA.</li> <li>4. Cross_VLAN bit in register 003E<sub>H</sub>.</li> </ol>
<b>ARP/RARP</b>	The cross_VLAN packet is determined in priority order by: <ol style="list-style-type: none"> <li>1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set.</li> <li>2. Cross-VLAN bit in register 000D<sub>H</sub>.</li> </ol>

**Table 13 Cross\_VLAN Packet** (cont'd)

Packet Type	Description
IGMP_IP/MLD_IP/MLD_IPV6	The cross_VLAN packet is determined in priority order by: 1. Cross-VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross-VLAN bit in register 000C <sub>H</sub> .
Others	The Cross_VLAN packet is determined in priority order by: 1. Cross_VLAN bit defined in the Special TAG, when Cross_VLAN_Valid is set. 2. Cross_VLAN bit defined in the learning table when there is a match for DA+FID.If the first and second conditions are not satisfied, the frame is classified as non-cross_VLAN packets.

### 3.1.14 Tagged VLAN or Port VLAN

The difference between two VLAN rules is the way to search the VLAN boundary. Users could enable “TAG Base VLAN” (see 0011<sub>H</sub>, [TBV](#)) bit to instruct Samurai-6M/6MX (ADM6996M/MX) to operate in the Tagged VLAN mode.

#### 3.1.14.1 VLAN Filters

Samurai-6M/6MX (ADM6996M/MX) supports 16 VLAN filters, each specifying a Valid bit, a TAG PRI, a VID, a FID, a Tagged Member, and a Member.

**Table 14 VLAN Filters**

VLAN Filter 0	VLAN_Valid	VLAN_PRI[2:0]	VID[11:0]	FID[3:0]	Tagged Member[5:0]	Member[5:0]
~						
VLAN Filter 15						

#### 3.1.14.2 Port VLAN

Port VLANs are created by grouping individual physical ports together. In this mode, only 6 VLAN filters (VLAN filter 0 ~5) are used. By the time examining the received frame, the source port is used as an index to search the VLAN filter. If the source port is port 0, then Member in the filter 0 is the VLAN group that port 0 joins.

#### 3.1.14.3 Tagged VLAN

Tagged VLAN is created with the aid of the VID in the packet or VID assigned by the source port. This VID is compared with 16 VIDs in the VLAN filters to check if any match exists. The Member in this matched filter is the VLAN boundary for the packet.

#### 3.1.14.4 VID for Comparison and Carried through Samurai-6M/6MX (ADM6996M/MX)

VID for comparison and carried through Samurai-6M/6MX (ADM6996M/MX) (as egress VID) depends on the VLAN configuration.

VID0: The incoming packet is tagged with VID = 000<sub>H</sub>. Enable “Replace VID0” (see 000A<sub>H</sub>, [RVID0](#)) to replace the Null VID with PVID (see basic control registers) if necessary.

VID1: The incoming packet is tagged with VID = 001<sub>H</sub>. Enable “Replace VID1” (see 000A<sub>H</sub>, [RVID1](#)) to replace VID1 with PVID (see basic control registers) if necessary.

VIDFFF: The incoming packet is tagged with VID = FFF<sub>H</sub>. Enable “Replace VIDFFF” (see 000A<sub>H</sub>, [RVIDFFF](#)) to replace VIDFFF with PVID (see basic control registers) if necessary.

VLAN Security Samurai-6M/6MX (ADM6996M/MX) ignores packet's VID and always uses PVID to see if there is a match and transfers it to the output ports. Disables the "VLAN Security Disable" (See 0022<sub>H</sub>, **VSD**) to achieve this goal.

Input Force No Tag when enabled (see 0020<sub>H</sub>, **IFNTE**), Samurai-6M/6MX (ADM6996M/MX) assumes all the packets are untagged and PVID is used. Input Force No Tag and VLAN Security are different in some situations.

**Table 15 VID Comparison**

Parameter	Tagged Frame with VID = 12'hfff	Packet Transmitted Tagged
<b>VLAN Security</b>	The frame is recorded as a VLAN violation and discarded if VIDFFF is not replaced.	Output packets have only one VLAN tag.
<b>Input Force No Tag</b>	The frame is recognized as an untagged frame. PVID is carried with this packet to the output port.	Output packets may have double tags, because the packet is transmitted with an additional tag with PVID.

### 3.1.14.5 Admit Only VLAN-Tagged Packets

Samurai-6M/6MX (ADM6996M/MX) supports a function to check if the packet is VLAN-Tagged, and any packets received on that port that carries no VID (untagged packets or packets with VID = 0) are discarded and recorded as a VLAN violation. This feature is implemented by programming the "Admit Only VLAN-Tagged" (see 0027<sub>H</sub>, **AOVTP**).

Samurai-6M/6MX (ADM6996M/MX) assumes all the packets are untagged in the "Input Force No Tag" mode and users should care that in this situation, "Admit Only VLAN Tagged" is of no effect.

### 3.1.14.6 VID Check

In Tagged VLAN, the VID for comparison must be contained in the VLAN filters, or the packet received on the port will be dropped and recorded as a VLAN violation. This feature is disabled by programming the "VID CHECK" bit to 0 (see 0026<sub>H</sub>, **VC**) to forward these packets instead of dropping them.

### 3.1.14.7 FID and VLAN Boundary

In Samurai-6M/6MX (ADM6996M/MX), every incoming packet is associated with a FID group. Samurai-6M/6MX (ADM6996M/MX) searches the learning table for the FID + DA, FID + SA. VLAN boundary restricts the allowable destination ports.

**Table 16 FID Search Algorithm**

Port VLAN	The source port number is the VLAN filter index. We can find FID in this filter.		
Tagged VLAN	VID match	Fid is contained in the matched filter. We can find FID in this filter.	
	VID un-match	VID check	The frame is dropped.
VID uncheck		Default FID is the FID (see 000A <sub>H</sub> , <b>DFID</b> ). If users configure Samurai-6M/6MX (ADM6996M/MX) to back to port VLAN (see 0027 <sub>H</sub> , <b>BPV</b> ), we can find the FID in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~ 15 are for VID comparison.	

**Table 17 VLAN Boundary Search Algorithm**

Port VLAN	The source port number is the VLAN filter index. We can find the boundary in this filter.
-----------	---

**Table 17 VLAN Boundary Search Algorithm (cont'd)**

Tagged VLAN	VID match	Member is contained in the matched filter. We can find the boundary in this filter	
	VID un-match	VID check	The frame is dropped.
		VID uncheck	Samurai-6M/6MX (ADM6996M/MX) uses Default VLAN Portmap as the boundary (see 003A <sub>H</sub> , <b>DVM</b> ). If users configure Samurai-6M/6MX (ADM6996M/MX) to “Back to Port VLAN” (see 0027 <sub>H</sub> , <b>BPV</b> ), we can back to find the boundary in the same way as the Port VLAN. When this feature is enabled, VLAN filter 0 ~ 5 are for Port VLAN purpose and VLAN filter 6 ~15 are for VID comparison.

### 3.1.14.8 Ingress Filter

If the source port is not contained in the VLAN boundary associated with the incoming packet, then this frame is dropped and recorded as a VLAN violation. This feature is disabled by setting the “Ingress Filter” (see 0021<sub>H</sub>, **IFE**) bit to 0<sub>B</sub>.

### 3.1.14.9 VLAN Violation

When packets are recorded as a VLAN violation packet, Samurai-6M/6MX (ADM6996M/MX) will drop them. The only way to ignore these violations is to classify these packets as cross\_VLAN packets.

### 3.1.14.10 TXTAG Carried through Samurai-6M/6MX (ADM6996M/MX)

Each packet during receive is assigned 2-bit TXTAG value. This value is carried by Samurai-6M/6MX (ADM6996M/MX) to the output ports to help to determine if egress tagged is necessary.

**Table 18 TXTAG Carried through Samurai-6M/6MX (ADM6996M/MX)**

Packet Type	Description
BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG in the learning table when there is a match for DA+FID in the learning table. 3. TXTAG in the control table when there is a match for DA in the control table. 4. TXTAG defined in register 003E <sub>H</sub> .
ARP/RARP	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 000D <sub>H</sub> .
IGMP_IP/MLD_IP/MLD_IPV6	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. TXTAG is defined in 000C <sub>H</sub> .
Other	The TXTAG is determined in priority order by: 1. TXTAG in Special Tag with TXTAG_Valid enabled. 2. The DA + FID matches an entry in the learning table with TXTAG defined.If the first and second conditions are not satisfied, TXTAG is 2'b00.

### 3.1.14.11 Tagged Member Carried through Samurai-6M/6MX (ADM6996M/MX)

If the output port is a tagged port it is determined by the port or the VID. Ports in the tagged members should egress packets tagged.



**First Way: New Transmit Tag Disable (see 0x000ah)**

The "Output Packet Tagging" bit in the basic control registers determines the tagged members.

**Second Way: New Transmit Tag Enable (see 0x000ah)**

Port VLAN	The source port number is the VLAN filter index. We can find the tagged member in this filter.		
Tagged VLAN	VID match	Tagged members are contained in the matched VLAN filter. We can find the tagged members in this filter	
	VID un-match	VID check	The frame is dropped.
VID uncheck		Samurai-6M/6MX (ADM6996M/MX) uses the first way to determine the tagged members. If users configure Samurai-6M/6MX (ADM6996M/MX) to "Back to Port VLAN" (see 0027 <sub>H</sub> , BPV), it can go back to find the tagged members in the same way as the Port VLAN.	

Users should note that when the Special Tag with Tagged Member Valid = 1<sub>B</sub> is incoming, the Samurai-6M/6MX (ADM6996M/MX) always uses Tagged Member in the Special Tag as the Tagged Member.

**3.1.14.12 Egress Tag Rule**

On the receiving port, Samurai-6M/6MX (ADM6996M/MX) will attach each packet with the tagged members by the Ingress rule. When the packet reaches the destination port, Samurai-6M/6MX (ADM6996M/MX) will check if the destination port is a tagged member, if yes, the packet will be transmitted tagged.

**Table 19 Egress Tag Result**

Untagged packets are received (If Input Force No Tag is enabled, Samurai-6M/6MX (ADM6996M/MX) assumes all the received packets are untagged.)	Output port is in the tagged members carried with the packet.	<p>TXTAG Description</p> <p>00<sub>B</sub> System Default Tag. Packets are transmitted tagged.</p> <p>01<sub>B</sub> Unmodified. Packets are transmitted untagged.</p> <p>10<sub>B</sub> Always Tagged. Packets are transmitted tagged.</p> <p>11<sub>B</sub> Always Untagged. Packets are transmitted untagged.</p>
	Output port is not in the tagged members carried with the packet.	<p>TXTAG Description</p> <p>00<sub>B</sub> System Default Tag. Packets are transmitted untagged.</p> <p>01<sub>B</sub> Unmodified. Packets are transmitted untagged.</p> <p>10<sub>B</sub> Always Tagged. Packets are transmitted tagged.</p> <p>11<sub>B</sub> Always Untagged. Packets are transmitted untagged.</p>
	Output port is configured to operate in the bypass mode. See 002A <sub>H</sub> .	<p>TXTAG Description</p> <p>00<sub>B</sub> System Default Tag. Packets are transmitted untagged.</p> <p>01<sub>B</sub> Unmodified. Packets are transmitted untagged.</p> <p>10<sub>B</sub> Always Tagged. Packets are transmitted tagged.</p> <p>11<sub>B</sub> Always Untagged. Packets are transmitted untagged.</p>

**Table 19 Egress Tag Result (cont'd)**

Tagged packets are received.	Output port is in the tagged members carried with the packet.	TXTAG Description 00 <sub>B</sub> System Default Tag. Packets are transmitted tagged. 01 <sub>B</sub> Unmodified. Packets are transmitted tagged. 10 <sub>B</sub> Always Tagged. Packets are transmitted tagged. 11 <sub>B</sub> Always Untagged. Packets are transmitted untagged.
	Output port is not in the tagged members carried with the packet.	TXTAG Description 00 <sub>B</sub> System Default Tag. Packets are transmitted untagged. 01 <sub>B</sub> Unmodified. Packets are transmitted tagged. 10 <sub>B</sub> Always Tagged. Packets are transmitted tagged. 11 <sub>B</sub> Always Untagged. Packets are transmitted untagged.
	Output port is configured to operate in the bypass mode. See 002A <sub>H</sub> .	TXTAG Description 00 <sub>B</sub> System Default Tag. Packets are transmitted tagged. 01 <sub>B</sub> Unmodified. Packets are transmitted tagged. 10 <sub>B</sub> Always Tagged. Packets are transmitted tagged. 11 <sub>B</sub> Always Untagged. Packets are transmitted untagged.

### 3.1.14.13 Tagged PRI Carried through Samurai-6M/6MX (ADM6996M/MX)

**Table 20 Tagged PRI Carried**

Untagged packets are received (If Input Force No Tag is enabled, Samurai-6M/6MX (ADM6996M/MX) assumes all the received packets are untagged.)	Port VLAN	[Change Priority Enable, Change Rule] (see 000A <sub>H</sub> , <a href="#">PCE&amp;PCR</a> ) 0x <sub>B</sub> Reverse PRI. 10 <sub>B</sub> VLAN_PRI field in the matched VLAN filter. 11 <sub>B</sub> Reverse PRI	
	Tagged VLAN	VID unmatch	Reverse PRI
		VID match	[Change Priority Enable, Change Rule] (see 000A <sub>H</sub> , <a href="#">PCE&amp;PCR</a> ) 0x <sub>B</sub> Reverse PRI. 10 <sub>B</sub> VLAN_PRI field in the matched VLAN filter. 11 <sub>B</sub> Reverse PRI

**Table 20 Tagged PRI Carried (cont'd)**

Tagged packets are received.	Port VLAN	[Change Priority Enable, Change Rule] (see 000A <sub>H</sub> , <b>PCE&amp;PCR</b> ) 0 <sub>B</sub> Tagged PRI = The 3-bit user priority in the tag header. 10 <sub>B</sub> VLAN_PRI field in the matched VLAN filter. 11 <sub>B</sub> Reverse PRI	
	Tagged VLAN	VID un-match	Change Priority Enable (see 000A <sub>H</sub> , <b>PCE</b> ) 0 <sub>B</sub> Tagged PRI = The 3-bit user priority in the tag header. 1 <sub>B</sub> Reverse PRI.
		VID match	[Change Priority Enable, Change Rule] (see 000A <sub>H</sub> , <b>PCE&amp;PCR</b> ) 0 <sub>B</sub> Tagged PRI = The 3-bit user priority in the tag header. 10 <sub>B</sub> VLAN_PRI field in the matched VLAN filter. 11 <sub>B</sub> Reverse PRI

Reserve PRI is reversed from the priority queue the packet is switched through.

Compare = queue, queue, queue, queue} XOR VLAN Priority MAP in 000E<sub>H</sub>.

Then we get Tagged PRI.

Compare Tagged PRI

XXXX\_XXX0<sub>B</sub> = 000<sub>B</sub>

XXXX\_XX01<sub>B</sub> = 001<sub>B</sub>

XXXX\_X011<sub>B</sub> = 010<sub>B</sub>

XXXX\_0111<sub>B</sub> = 011<sub>B</sub>

XXX0\_1111<sub>B</sub> = 100<sub>B</sub>

XX01\_1111<sub>B</sub> = 101<sub>B</sub>

X011\_1111<sub>B</sub> = 110<sub>B</sub>

0111\_1111<sub>B</sub> = 111<sub>B</sub>

1111\_1111<sub>B</sub> = 000<sub>B</sub>

### 3.1.14.14 CFI Carried through Samurai-6M/6MX (ADM6996M/MX)

**Table 21 CFI Carried**

<b>CFI Carried</b>	
Untagged frames received (If Input Force No Tag is enabled, Samurai-6M/6MX (ADM6996M/MX) assumes all the received packets are untagged.)	CFI Carried = 0 <sub>B</sub>
Tagged frame received	CFI Carried = Original CFI in the tag header.

### 3.1.14.15 Egress TAG

Egress tag contains Egress PRI, Egress CFI, and Egress VID. When packets are transmitted tagged, this egress tag associated with Ethernet-Type = 8100<sub>H</sub> is inserted following the Ethernet source address.

Egress PRI: Egress PRI is Tagged PRI carried through Samurai-6M/6MX (ADM6996M/MX) from the source port.

Egress CFI: Egress CFI is CFI carried through Samurai-6M/6MX (ADM6996M/MX) from the source port.

Egress VID: Egress VID is VID carried through Samurai-6M/6MX (ADM6996M/MX) from the source port.

### 3.1.15 Priority Queue

Samurai-6M/6MX (ADM6996M/MX) supports 4 priority queues and each is assigned a weight.

**Table 22 Priority Queue**

Queue	Weight
Queue 0	Weight = 1
Queue 1	Weight = "Queue 1 Weight" bits in 0025 <sub>H</sub>
Queue 2	Weight = "Queue 2 Weight" bits in 0026 <sub>H</sub>
Queue 3	Weight = "Queue 3 Weight" bits in 0027 <sub>H</sub>

### 3.1.15.1 System PRI

The system PRI is determined in the order as follows:

- (DA+FID) was found in the learning table, then LRN\_PRI field (when LRN\_PRIEN is set) in this entry indicates the priority queue.
- Port PRI in basic control register indicates the priority queue, when Port\_PRIEN is enabled on that port.
- The user priority field in the tag header is used for a tagged packet ("Input Force No Tag" doesn't effect Samurai-6M/6MX (ADM6996M/MX) to extract the PRI in the tag header), when "VLAN Priority" is enabled. The user priority in the tag header is a 3 bits field, Samurai-6M/6MX (ADM6996M/MX) uses "VLAN Priority MAP" to map the priority queue.
- For IP packets with no tag header, IP PRI is used when "Service Priority" (see 001F<sub>H</sub>) is enabled. Even for a tagged packet with IP header, we can set "IP over VLAN" (see basic control registers) bit to 1 to force using IP PRI. Three kinds of IP PRI are available.
  - For IPV6 packets with IP Version = 6<sub>H</sub>, the most significant 6 bits of the traffic class in the IPV6 header is used to map the priority queue by the service mapping registers.
  - For IPV4 packets with IP Version = 4<sub>H</sub>, the most significant 3 bits of the TOS field in the IPV4 header is used to map the priority queue by the TOS Priority Map register.
  - If "TOS Using" (see 000A<sub>H</sub>) is disabled, even for IPV4 packets, Samurai-6M/6MX (ADM6996M/MX) uses the most significant 6 bits of the TOS field to map the priority queue by the service mapping registers.
- If the packet matches the TCP/UDP filters, the PRI associated with this filter indicates the priority queue when "TCP/UDP PRIEN" is set to 1 (see 0098<sub>H</sub>). Users could enable "TCPUDP over IP" to force using the TCPUDP PRI when there is a match.

### 3.1.15.2 Queue Assigned

**Table 23 Queue Assigned**

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)	The Order of Priority Assigned
BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3	<ol style="list-style-type: none"> <li>The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue.</li> <li>If (DA+FID) matches an entry in the learning table, then LRN_PRI field with LRN_PRIEN enabled in this entry indicates the priority queue.</li> <li>Use PRI in 003D<sub>H</sub> to indicate the queue the frame was switched.</li> </ol>
ARP/RARP	<ol style="list-style-type: none"> <li>The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue.</li> <li>Use PRI in 000D<sub>H</sub> to indicate the priority queue when enabled.</li> <li>Use System PRI.</li> </ol>

**Table 23 Queue Assigned (cont'd)**

<b>Packets Identified by Samurai-6M/6MX (ADM6996M/MX)</b>	<b>The Order of Priority Assigned</b>
IGMP_IP/MLD_IP/MLD_IPV6	<ol style="list-style-type: none"> <li>1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue.</li> <li>2. Use PRI in 000C<sub>H</sub> to indicate the priority queue when enabled.</li> <li>3. Use System PRI.</li> </ol>
Others	<ol style="list-style-type: none"> <li>1. The PRI field with PRI_Valid = 1 in the Special TAG indicates the priority queue.</li> <li>2. Use System PRI.</li> </ol>

### 3.1.15.3 Configure Samurai QoS Function

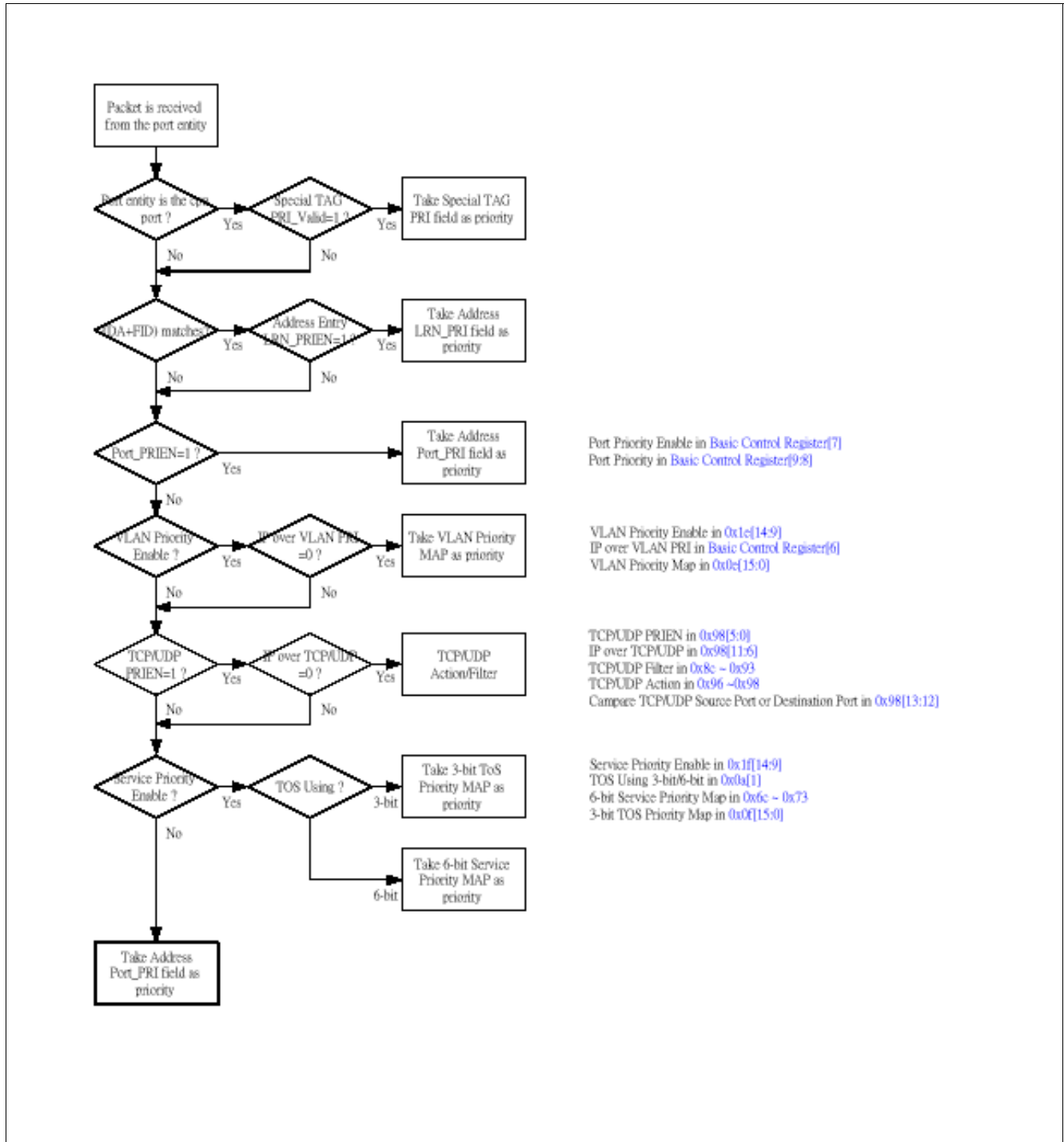


Figure 5 To Configure Samurai QoS Function

### 3.1.16 Address Learning

Samurai-6M/6MX (ADM6996M/MX) provides two ways to create the entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow the maximum of 4 different addresses with the same hash key to be stored at the same time. Up to 2k entries can be created and all entries are stored

in the internal SSRAM. Samurai-6M/6MX (ADM6996M/MX) searches the learning table for the SA+FID of the incoming packet or the instruction from CPU. When both fields (a single SA may exist in different FID) are matched, there is a match.

### 3.1.16.1 Dynamic Learning

The Samurai-6M/6MX (ADM6996M/MX) searches for SA and FID of an incoming packet in the address table and takes dynamic learning action as follows:

1. If (SA+FID) was not found in the learning table, create a new entry with SA, FID, and the incoming port.
2. If (SA+FID) was found in the learning table, and the incoming port and the Portmap doesn't match, create a new entry with SA, FID, and the incoming port.

Dynamic learning will be disabled in the following condition:

1. Security violation exists on the port.
2. VLAN violation exists on the port.
3. The packet is a PAUSE packet.
4. The number of the addresses that port has learned has reached its maximum.
5. The port disables its learning function (see extended control registers).
6. The packet is an illegal packet (too long, too short or FCS error).
7. A packet with Special Tag is received and the LRN bit is 0 and LRN\_Valid = 1<sub>B</sub>.
8. The port is in the Disabled state in the Spanning Tree Protocol.
9. The port is in the Blocking/Listening state in the Spanning Tree Protocol.
10. All the four entries in the same hash address are occupied and all of them are static addresses.

### 3.1.16.2 Manual Learning

The Samurai-6M/6MX (ADM6996M/MX) implements the manual learning through the CPU's help. The CPU can create or remove any entry in the address table. Each entry could be static. "Static" means the entry will not be aged forever. When the entry is static, then the definition in some fields is modified to make Samurai-6M/6MX (ADM6996M/MX) work more flexibly.

### 3.1.16.3 Learning Table

#### 3.1.16.3.1 Entry Format in the Learning Table

<b>69</b>	<b>68</b>	<b>67</b>	<b>66 ... 58</b>	<b>57 ... 52</b>	<b>51 ... 48</b>	<b>47 ... 0</b>
Bad	Info_Type	Occupy	Info_Ctrl/Age Timer	Portmap	FID	Address

Field	Description
Bad	The entry is marked to show if it is failed during the learning table memory bist time. 0 <sub>B</sub> Don't fail 1 <sub>B</sub> Fail
Info_Type	Static Address. 0 <sub>B</sub> The entry is not static 1 <sub>B</sub> The entry is static

Function Description

Field	Description	
Occupy	The entry is marked to show the status if the entry is occupied. 0 <sub>B</sub> Don't occupy 1 <sub>B</sub> Occupy	
Info_Ctrl/Age Timer	Info_Ctrl is used when the entry is static.	
	Bit	Description
	8	Source Intrusion 0 <sub>B</sub> It isn't a violated source address 1 <sub>B</sub> It is a violated source address
	7	Span 0 <sub>B</sub> Not a span packet 1 <sub>B</sub> A span packet
	6	Management 0 <sub>B</sub> Not a management packet 1 <sub>B</sub> A management packet
	5	Cross_VLAN 0 = Not a cross_VLAN packet. 1 = A cross_VLAN packet.
	4:3	TXTAG It is used as an option for inserting Tag on the transmission port. 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
	2	LRN_PRIEN 0 <sub>B</sub> LRN_PRI is not used 1 <sub>B</sub> LRN_PRI is used
	1:0	LRN_PRI It identifies the address priority. 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
		Age Timer is used when the entry is not static.
	Bit	Description
	8:0	Age Timer This timer is used to control the ageing time.
Portmap	The field is used as the output ports associated with the FID+MAC Address.	
FID	The field is used as the FID group associated with the MAC address.	
Address	The MAC Address in the learning table.	

### 3.1.16.3.2 The Registers Accessing the Learning Table

12 registers are provided by Samurai-6M/6MX (ADM6996M/MX) to support access to the address table. These 12 registers are Address Table Control Register 0 ~ 5 and Address Table Status Register 0 ~ 5 in 011A<sub>H</sub> ~ 0125<sub>H</sub>.



**Table 24 Control Register Description for Accessing the Address Table**

Command	Access Control	Info_Type	Info_Ctrl/Age Timer	Portmap	FID	Address
Control 5[6:4]	Control 5[3:0]	Control 4[12]	Control 4[8:0]	Control 3[9:4]	Control 3[3:0]	{Control 2, Control 1, Control 0}

The Address, FID, Portmap, Info\_Ctrl/Age Timer and Info\_Type in the Control Register have the same meaning as those in the entry format. The Command and Access Control are described as follows:

**Table 25 Description for Command and Access Control**

Command	Access Control	Description
000 <sub>B</sub>	0111 <sub>B</sub>	Create a new address
000 <sub>B</sub>	1111 <sub>B</sub>	Overwrite an existed address
001 <sub>B</sub>	1111 <sub>B</sub>	Erase an existed address
010 <sub>B</sub>	0000 <sub>B</sub>	Search an empty address
010 <sub>B</sub>	1001 <sub>B</sub>	Search by the port in the Output Port field
010 <sub>B</sub>	1010 <sub>B</sub>	Search by the forwarding group specified in the Forwarding Group field
010 <sub>B</sub>	1100 <sub>B</sub>	Search by the address specified in the MAC Address field
010 <sub>B</sub>	1110 <sub>B</sub>	Search by the address and forwarding group
010 <sub>B</sub>	1101 <sub>B</sub>	Search by the address and output port
010 <sub>B</sub>	1011 <sub>B</sub>	Search by the forwarding group and the output port
010 <sub>B</sub>	1111 <sub>B</sub>	Search by the address, the forwarding group and the output port
011 <sub>B</sub>	0100 <sub>B</sub>	Initial to location by the address field
011 <sub>B</sub>	0000 <sub>B</sub>	Initial to the first address

**Table 26 Status Register Description**

Busy	Result	Bad	Occupy	Info_Type	Info_Ctrl/Age_Time	Portmap	FID	Address
Status 5 [15]	Status 5 [14:12]	Status 5 [2]	Status 5 [1]	Status 5 [0]	Status 4 [8:0]	Status 3 [9:4]	Status 3 [3:0]	{Status 2, Status 1, Status 0}

**Table 27 Description for the Status Register**

Address	If the search operation is successful, the switch will return the MAC address in this field. If the search fails, this field doesn't mean anything.
FID	If the search operation is successful, the switch will return FID in the matched entry.
Portmap	If the search operation is successful, the switch will return Portmap in the entry.
Info_Ctrl/Age Time	If the search operation is successful, the switch will return Info_Ctrl/Age Timer in the entry.
Info_Type	If the search operation is successful, the switch will return Info_Type in the entry
Occupy	If the search operation is successful, the switch will return Occupy in the entry
Bad	If the search operation is successful, the switch will return Bad in the entry

**Table 27** Description for the Status Register (cont'd)

Result	<p>This field tells us the status for not only the search operation but also the creating operation.</p> <p>000<sub>B</sub> Command OK</p> <p>001<sub>B</sub> All Entry Used. This result happens only for the create operation. Samurai-6M/6MX (ADM6996M/MX) uses the 4-way address lookup engine so it allows 4 different addresses stored at each hash location. If these 4 entries are all static, then CPU will not successfully create 5 different addresses hashed to the same location and 001 will be returned. The only way to create 5 different addresses is to remove one of earlier addresses.</p> <p>101<sub>B</sub> Command Error</p>
Busy	<p>This bit indicates if the table engine for access is available.</p> <p>1<sub>B</sub> The engine is busy and it will not accept the command from the CPU.</p> <p>0<sub>B</sub> The engine is available.</p>

### 3.1.16.3.3 Rules to Access the Learning Table

1. Check the Busy Bit in the status register to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write the MAC address[15:0] into the control register 0.
3. Write the MAC address[31:16] into the control register 1.
4. Write the MAC address[47:32] into the control register 2.
5. Write the Portmap and FID into the control register 3.
6. Write the Info\_Ctrl/Age Timer and Info\_Type into the control register 4.
7. Write the Access Control and Command into the control register 5 to define the operation.
8. Wait for the engine to complete (Check the Busy Bit).
9. Read the desired result returned in the status register.

*Note: Before a new search starts, the CPU should execute the "Initial command" to initial the search pointer. The search engine could search the aim from the top to the bottom. The search engine has an ability to move the pointer to the associated location automatically (The result will be returned). Because more than one entry may match the searching condition (by port, by address, etc.) at the same time, the CPU should continue to restart the search engine until the Command Result = Entry Not is found to confirm that no other matching entries exist and at this time a new search can be started.*

### 3.1.16.3.4 Example

Example	Rule
The user needs Samurai-6M/6MX (ADM6996M/MX) to forward the specified unicast packet (DA = 0012-3456-789A <sub>H</sub> and FID = 2) to port 3 forever.	<ol style="list-style-type: none"> <li>1. Check the Busy bit. If Busy = 0<sub>B</sub>, go to the next step. If Busy = 1<sub>B</sub>, wait.</li> <li>2. Write 789A<sub>H</sub> into control register 0.</li> <li>3. Write 3456<sub>H</sub> into control register 1.</li> <li>4. Write 0012<sub>H</sub> into control register 2.</li> <li>5. Write 0082<sub>H</sub> into control register 3.</li> <li>6. Write 1000<sub>H</sub> into control register 4.</li> <li>7. Write 0007<sub>H</sub> into control register 5.</li> <li>8. Read the status register 5 to check the busy bit. If Busy = 0<sub>B</sub>, check the Command Result to see if the create operation is successful. If Busy = 1<sub>B</sub>, wait</li> </ol>
The user needs Samurai-6M/6MX (ADM6996M/MX) to forward the specified multicast packet (DA = 0123-4567-89AB <sub>H</sub> and FID = 3) to port 0, and port 1 both. This address could be aged.	<ol style="list-style-type: none"> <li>1. Check the Busy bit. If Busy = 0<sub>B</sub>, go to the next step. If Busy = 1<sub>B</sub>, wait.</li> <li>2. Write 89AB<sub>H</sub> into control register 0.</li> <li>3. Write 3456<sub>H</sub> into control register 1.</li> <li>4. Write 0123<sub>H</sub> into control register 2.</li> <li>5. Write 0033<sub>H</sub> into control register 3.</li> <li>6. Write 0000<sub>H</sub> into control register 4.</li> <li>7. Write 0007<sub>H</sub> into control register 5.</li> <li>8. Read the status register 5 to check the busy bit. If Busy = 0<sub>B</sub>, check the Command Result to see if the create operation is successful. If Busy = 1<sub>B</sub>, wait</li> </ol>
The user wants to know how many stations attached to port 4	<ol style="list-style-type: none"> <li>1. Check the Busy bit. If Busy = 0<sub>B</sub>, go to the next step. If Busy = 1<sub>B</sub>, wait.</li> <li>2. Write 0030<sub>H</sub> into control register 5 to initial the search pointer to the first address.</li> <li>3. Wait until the Busy bit changes to 0<sub>B</sub>.</li> <li>4. Write 0100<sub>H</sub> into the control register 3.</li> <li>5. Write 0029<sub>H</sub> into the control register 5 to start the operation of the search by port.</li> <li>6. Read the status register 5 to check the busy bit. If Busy = 0<sub>B</sub>, check the Command Result to see if the search operation is successful (the Mac address attached to port 4 could be derived from the MAC address in the status register). If Busy = 1<sub>B</sub>, wait for completion.</li> <li>7. If Command Result = "Command OK", it means some other MAC addresses attached to port 4 may exist. We should restart the "Search by port" command again to let the search engine look after another addresses.</li> <li>8. If the Command Result = "Entry Not Found", it means no other addresses attached to port 4 exist.</li> </ol>

### 3.1.17 Hardware Based IGMP Snooping

Samurai-6M/6MX (ADM6996M/MX) supports IGMP v1/v2 Snooping without any software effort. Samurai-6M/6MX (ADM6996M/MX) will monitor the IGMP traffic and update its embedded IGMP membership table if the hardware based IGMP snooping function is enabled. IP multicast frames can be forwarded according to the Port-Map information of the membership table. The data of the membership can also be accessed by the CPU via SDC/SDIO interface. The following registers could be used to configure the IGMP Snooping behavior.

1. EEPROM register 00B<sub>H</sub> bit [13:12], Additional Snooping Control register.ports.
2. EEPROM register 00B<sub>H</sub> bit [2], Source Violation Over Snooping.
3. EEPROM register 00B<sub>H</sub> bit [1], Source Violation Over Default.
4. EEPROM register 00C<sub>H</sub> bit [13:6], various Snooping Control registers.
5. EEPROM register 00C<sub>H</sub> bit [2], Hardware IGMP Packet Ignore CPU Port.
6. EEPROM register 00C<sub>H</sub> bit [1], Hardware IGMP Snooping Enable.

7. EEPROM register 00C<sub>H</sub> bit [0], Hardware IGMP Default Router Enable.
8. EEPROM register 00D<sub>H</sub> bit [14], IP Multicast Packet Treated as Cross VLAN packet.
9. EEPROM register 01B<sub>H</sub> bit [14:9], Multicast Port-Map.
10. EEPROM register 03F<sub>H</sub> bit [15:8], Query Interval.
11. EEPROM register 03F<sub>H</sub> bit [7:6], Robust Variable.
12. EEPROM register 03F<sub>H</sub> bit [5:0], Default Router Port-Map.

### 3.1.17.1 Entry Format of IGMP Membership Table

<b>57</b>	<b>56</b>	<b>55 ... 48</b>	<b>47 ... 42</b>	<b>41 ... 30</b>	<b>29</b>	<b>28... 23</b>	<b>22 ... 0</b>
Bad	Occupy	Reserved	Reserved	Reserved	Reserved	Portmap	Group ID

Field	Description
Bad	The entry is marked to show if it is failed during the memory BIST time of IGMP membership table. 0 <sub>B</sub> Doesn't fail 1 <sub>B</sub> Fail
Occupy	The entry is marked to show the status if the entry is occupied. 0 <sub>B</sub> Empty Entry 1 <sub>B</sub> Occupied Entry
Reserved	Reserved. Ignore the content in reading and fill in 0 in writing.
Reserved	Reserved. Ignore the content in reading and fill in 0 in writing.
Reserved	Reserved. Ignore the content in reading and fill in 0 in writing.
Reserved	Reserved. Ignore the content in reading and fill in 0 in writing.
Portmap	This flag is used to denote whether the port is the member of this Group or not. 0 <sub>B</sub> The port is not the member of this Group. 1 <sub>B</sub> The port is the member of this Group.
Group ID	IP Multicast Group ID.

### 3.1.17.2 The Registers Accessing the IGMP Membership Table

The registers for accessing the IGMP membership table are the same with accessing MAC address filtering table, but the data format are re-defined as below.

**Table 28 Control Register Description for Accessing the IGMP Membership Table**

Command	Entry Address	Entry Data
Control 5[6:4]	Control 4[4:0]	{Control 3[9:0], Control 2, Control 1, Control 0}

The Command used to access IGMP membership table is defined as below.:

**Table 29 Description for Command and Access Control**

Command	Description
100 <sub>B</sub>	Write data into internal IGMP table
101 <sub>B</sub>	Read data from internal IGMP table

**Table 30 Entry Format of IGMP Membership Table**

Busy	Result	Entry Address	Entry Data
Status 5[15]	Status 5[14:12]	Status 4[4:0]	{Status 3[9:0], Status 2, Status 1, Status 0}

### 3.1.17.3 IGMP Snooping Introduction

IGMP snooping is a feature that allows the switch to “listen in” on the IGMP conversation between hosts and routers. When a switch hears an IGMP report from a host for a given multicast group, the switch adds the host’s port number to the GDA (Group Destination Addresses) list for that group. And, when the switch hears an IGMP leave, it removes the host’s port from the Multicast table entry.

#### Multicast Address

1. Multicast IP addresses are Class D IP addresses. Therefore, all IP addresses from 224.0.0.0 to 239.255.255.255 are multicast IP addresses. They are also referred to as Group Destination Addresses (GDA).

2. For each GDA there is an associated MAC address. This MAC address is formed by 01-00-5e, followed by the last 23 bits of the GDA translated in hex. Therefore:

- 230.20.20.20 corresponds to MAC 01-00-5e-14-14-14
- 224.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a

Consequently, this is not a one-to-one mapping, but a one-to-many mapping:

- 224.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a
- 226.10.10.10 corresponds to MAC 01-00-5e-0a-0a-0a, as well

3. Some Multicast IP addresses are reserved for special use. For example:

- 224.0.0.1 - All multicast-capable hosts.
- 224.0.0.2 - All multicast-capable routers
- 224.0.0.5 and 224.0.0.6 is used by: Open Shortest Path First (OSPF).

In general, addresses from 224.0.0.1 to 224.0.0.255 are reserved and used by various protocols.

#### IGMP

IGMP is a standard defined in RFC1112 for IGMPv1 and in RFC2236 for IGMPv2. It specifies how a host can register a router to receive specific multicast traffic.

#### IGMPv1

- **Membership Query** are issued by router at regular intervals to check whether there is still a host interested in the GDA in that segment.

**Table 31 IPV4/IGMP/General Query**

DA 01005e000001	SA 6 bytes	Type 16’h0800	Ver 4’h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8’h02	Unused 6 bytes	DIP 224.0.0.1
Unused (Len*4-20) bytes	TP 8’h11	Unused 3 bytes	GA 32’b0						

- **Membership Report** is issued by hosts that want to receive a specific multicast group (GDA). Host membership reports are issued either unsolicited (when the host wants to receive GDA traffic first) or in response to a membership query.

**Table 32 IPV4/IGMP/V1 Report**

DA 01005exxxxxx	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 4 bytes
Unused (Len*4-20) bytes	TP 8'h12	Unused 3 bytes	GA 4 bytes						

Host membership queries are sent by router to the all multicast address: 224.0.0.1. These queries use 0.0.0.0 in the IGMP GDA field. A host for each group must respond to that query or the router will stop forwarding the traffic for that GDA to that segment (after 3 attempts). The router simply keeps a multicast routing entry for each source and links it to a list of outgoing interfaces (interface from where the IGMP report came). After three IGMP query attempts with no answer, this interface is erased from outgoing interface list for all entries linked to that GDA.

*Note: IGMPv1 has no leave mechanism. If a host no longer wants to receive the traffic, it simply quits. If it is the last, the router will not have any answers to its query and will delete the GDA for that subnet.*

### IGMPv2

- Membership Query

**Table 33 IPV4/IGMP/General Query**

DA 01005e000001	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 224.0.0.1
Unused (Len*4-20) bytes	TP 8'h11	Unused 3 bytes	GA 32'b0						

- IGMPv1 Membership Report

**Table 34 IPV4/IGMP/V1 Report**

DA 01005exxxxxx	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 4 bytes
Unused (Len*4-20) bytes	TP 8'h12	Unused 3 bytes	GA 4 bytes						

- IGMPv2 Membership Report

**Table 35 IPV4/IGMP/V2 Report**

DA 01005exxxxxx	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 4 bytes
Unused (Len*4-20) bytes	TP 8'h16	Unused 3 bytes	GA 4 bytes						

- **Leave Group** when a host wants to leave a group, it should send a Leave Group IGMP message to destination 224.0.0.2 (instead of leaving silently like in IGMPv1)

**Table 36 IPV4/IGMP/V2 Leave**

DA 01005000002	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 224.0.0.2
Unused (Len*4-20) bytes	TP 8'h17	Unused 3 bytes	GA 4 bytes						

- **Group-specific Query** a router can now send a group-specific query by sending a Membership Query to the group GDA instead of sending it to 0.0.0.0

**Table 37 IPV4/IGMP/Group-Specific Query**

DA 01005exxxxxx	SA 6 bytes	Type 16'h0800	Ver 4'h4	Len 4 bits	TOS 1 byte	Unused 7 bytes	Protocol 8'h02	Unused 6 bytes	DIP 4 bytes
Unused (Len*4-20) bytes	TP 8'h11	Unused 3 bytes	GA 4 bytes						

### Learning the Router Port

The switch listens to the following messages in order to detect router ports with IGMP snooping

- IGMP Membership query send to 01-00-5e-00-00-01

Once a router port is detected, it is added to the port list of all GDAs in that VLAN.

[Hardware IGMP Snooping]

1. Enable Hardware IGMP Snooping, set EEPROM register 0C<sub>H</sub>[1]=1

2. Hardware IGMP Default Router

- If EEPROM register 0C<sub>H</sub>[0]=0, Samurai will learn the router port automatically.

*Note: The presence of the router port is configured by Query Interval (EEPROM register 3F<sub>H</sub>[15:8]) defined as the length of time that must pass before the Router Port decides there is no longer another multicast router which should be the querier.*

- If EEPROM register 0C<sub>H</sub>[0]=1, Samurai will learn the router port according to the Default Router Port-map.
- If EEPROM register 3F<sub>H</sub>[5:0], Default Router Port-map

*Note: The router port always exists even no IGMP query is received. The group membership is maintained by Robust Variable (EEPROM register 3F<sub>H</sub>[7:6]) defined as the amount of query that must pass before the Default Router decides there are no members of a group on a network.*

### Joining a Group with IGMP Snooping

Below are two joining scenarios.

Scenario A: Host A is the first host to join a group in the segment.

- Host A sends an unsolicited IGMP Membership report.
- The switch intercepts the IGMP membership report that sent by the host that wanted to join the group.
- The switch creates a multicast entry for that group and links it to the port on which it has received the report and to all router ports.
- The switch forwards the IGMP report on to all router ports. This is so that the router will also receive the IGMP report and will update its multicast routing table accordingly.

[Hardware IGMP Snooping]

Samurai supports 32 IGMP membership table. Samurai will maintain IGMP membership table according to IGMPv1/v2 protocol. If 32 IGMP membership table is full, the later incoming IGMP packets will follow "Multicast Port-map".

User can use Address Table Control Register command and Address Table Status Register command to access 32 IGMP membership table.

**Table 38 IGMP Membership Table**

Address Table Control 0	EEPROM register 11A <sub>H</sub>	Address Table Status 0	EEPROM register 120 <sub>H</sub>
Address Table Control 1	EEPROM register 11B <sub>H</sub>	Address Table Status 1	EEPROM register 121 <sub>H</sub>
Address Table Control 2	EEPROM register 11C <sub>H</sub>	Address Table Status 2	EEPROM register 122 <sub>H</sub>
Address Table Control 3	EEPROM register 11D <sub>H</sub>	Address Table Status 3	EEPROM register 123 <sub>H</sub>
Address Table Control 4	EEPROM register 11E <sub>H</sub>	Address Table Status 4	EEPROM register 124 <sub>H</sub>
Address Table Control 5	EEPROM register 11F <sub>H</sub>	Address Table Status 5	EEPROM register 125 <sub>H</sub>

- IGMP membership table Read Command
  - (1) Check the **Busy** Bit in the **Status Register 5 [15]** to see if the access engine is available. If **Busy = 1<sub>B</sub>**, wait until the engine is free. If **Busy = 0<sub>B</sub>**, go to the following step.
  - (2) Write **Control Register 4 [4:0]** to assign the entry numbers you want to access.
  - (3) Write **Control Register 5 [6:4] = 101<sub>B</sub>** to start the operation of Read command.
  - (4) Read the **Busy** Bit in the **Status Register 5 [15]** to see if the operation is successful. If **Busy = 1<sub>B</sub>**, wait until the operation is completed. If **Busy = 0<sub>B</sub>**, read **Status Register 5 ~ 0** to get the IGMP membership table entry.
- IGMP membership table Write Command
  - (1) Check the **Busy** Bit in the **Status Register 5 [15]** to see if the access engine is available. If **Busy = 1<sub>B</sub>**, wait until the engine is free. If **Busy = 0<sub>B</sub>**, go to the following step.
  - (2) Write **Control Register 0 ~ 4** to assign the entry numbers you want to access.
  - (3) Write **Control Register 5 [6:4] = 100<sub>B</sub>** to start the operation of Write command.
  - (4) Read the **Busy** Bit in the **Status Register 5 [15]** to see if the operation is successful. If **Busy = 1<sub>B</sub>**, wait until the operation is completed. If **Busy = 0<sub>B</sub>**, read **Status Register 5 ~ 0** to get the IGMP membership table entry.

### 3.1.18 Address Aging

Samurai-6M/6MX (ADM6996M/MX) maintains an age timer for each address. The aging timer is reset to 0 when the packet is received. When aging time counts up to 300 seconds, it means that station didn't transmit packets in this period and the address can be removed from the table. This could help to prevent a station which leaves the network and occupies a table space for a long time. Aging function can be disabled from the EEPROM (see extend control registers) and if the address is static, then Samurai-6M/6MX (ADM6996M/MX) will not age it out either. The default aging timer is 300 seconds. User could change Aging Timer Select (0011<sub>H</sub>, **ATS**) to shorten the aging time.

### 3.1.19 Source Violation

Source violation is defined in Samurai-6M/6MX (ADM6996M/MX) to support flexible security modes. See Security Option in the EEPROM Basic Register and the Src\_Violation bit in the Learning Table.



**Function Description**

<b>Security Mode</b>	<b>Description</b>
First Lock	<p>Samurai-6M/6MX (ADM6996M/MX) locks the first SA+FID of packets received on the port. After the first (SA+FID) is locked, Samurai-6M/6MX (ADM6996M/MX) starts to check packets with different (SA+FID).</p> <ol style="list-style-type: none"> <li>1. If the packets are not assigned as management, drop it (modify the forwarding algorithm) and record it as a source violation.</li> <li>2. If the packets are management packets, and Source Violation (see 000B<sub>H</sub>, <b>System Control Register 1</b>) is configured to 1<sub>B</sub> for different kinds of packets, then Samurai-6M/6MX (ADM6996M/MX) modifies the forwarding algorithm to drop these packets. They are also recorded as a source violation.</li> <li>3. If the packets are management packets and Source Violation is configured to 0<sub>B</sub>, then Samurai-6M/6MX (ADM6996M/MX) doesn't modify the forwarding algorithm. In this situation, we don't record this case as a source violation.</li> </ol>
First Link Lock	<p>The first received packets will be locked as First Lock. The difference is that the receiving port will not receive and learn packets any more after the port links down even if it links up again. A source violation is recorded as the First Lock. If Samurai-6M/6MX (ADM6996M/MX) modifies the forwarding algorithm it is still as the First Lock.</p>
Assign Lock	<p>Samurai-6M/6MX (ADM6996M/MX) allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. A source violation is recorded as the First Lock. If Samurai-6M/6MX (ADM6996M/MX) modifies the forwarding algorithm it is still as the First Lock.</p>
Assign Link Lock	<p>Samurai-6M/6MX (ADM6996M/MX) allows users to assign the locked SA+FID through CPU's help instead of the first SA+FID. The others are the same as the First Link Lock.</p>
Discard Unknown	<p>The "unknown source address" means that (SA+FID) is not found in the learning table or even is found but Portmap doesn't match the incoming port. If "unknown" packets are received, Samurai-6M/6MX (ADM6996M/MX) records the source violation as the First Lock. The rule to modify the forwarding algorithm is still as the First Lock.</p>
Unknown to CPU	<p>This option is the same as "Discard Unknown" except that if Samurai-6M/6MX (ADM6996M/MX) decides to modify the forwarding algorithm, it will forward the packets to the CPU port instead of dropping them.</p>
Source Intrusion	<p>If the incoming port receives the packets with SA, marked as Source Intrusion, we handle these packets in the following rule:</p> <ol style="list-style-type: none"> <li>1. Enabled Source Intrusion Must (see 000B<sub>H</sub>, <b>SIM</b>) to instruct Samurai-6M/6MX (ADM6996M/MX) to modify the forwarding algorithm and record the source violation always.</li> <li>2. If Source Intrusion Must is not enabled, Samurai-6M/6MX (ADM6996M/MX) also modifies the forwarding algorithm and records the source violation when any non-management packets are received.</li> <li>3. If Source Intrusion Must is not enabled, Samurai-6M/6MX (ADM6996M/MX) also modifies the forwarding algorithm and records the source violation when management packets are received but Source Violation is configured to 1<sub>B</sub>.</li> <li>4. If Source Intrusion Must is not enabled, Samurai-6M/6MX (ADM6996M/MX) doesn't modify the forwarding algorithm and records the source violation when management packets are received and Source Violation is configured to 0<sub>B</sub>.</li> </ol> <p>Samurai-6M/6MX (ADM6996M/MX) allows the users to redirect the packets to the CPU port instead of dropping it when they violate the source intrusion (see Source Intrusion Action in 000B<sub>H</sub>, <b>SIA</b>).</p>

Samurai-6M/6MX (ADM6996M/MX) supports stricter security protection. The port is disabled when there is a source violation. Enable Security Option[3] to enable this feature.

### 3.1.20 Packet Forwarding

Samurai-6M/6MX (ADM6996M/MX) identifies packet headers and transfers it from the incoming port to the destination ports.

#### 3.1.20.1 Control Table

Samurai-6M/6MX (ADM6996M/MX) provides a control table for user to control the forwarding algorithm of the DA = 01 80 C2 00 00 00<sub>H</sub> ~ DA = 01 80 C2 00 00 2F<sub>H</sub> easily. This control table is defined in 0074<sub>H</sub> ~ 008B<sub>H</sub>.

#### 3.1.20.2 Default Output Ports

The default output ports that a packet is transferred to are determined in the following order.

1. The Portmap in the Special Tag with Portmap\_Valid = 1 is used as the output ports.
2. The Portmap in the learning table is used as the output ports, when (DA+FID) matches an entry in the learning table.
3. The Portmap in the hardware IGMP table is used as the output ports, when DA matches an entry in the hardware IGMP table and “Hardware IGMP Snooping” (see 000C<sub>H</sub>, **HISE**) is enabled.
4. “Broadcast Portmap” (see 001A<sub>H</sub>, **BP**) is used as the output ports, when the incoming packet is a broadcast packet.
5. “Multicast Portmap” (see 001B<sub>H</sub>, **MP**) is used as the output ports, when the incoming packet is a multicast packet.
6. “Unicast Portmap” (see 0019<sub>H</sub>, **UP**) is used as the output ports, when the incoming packet is a unicast packet.

#### 3.1.20.3 Forwarding Algorithm

Table 39 Forwarding Algorithm

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)	Algorithm
BPDU/SLOW/PAE/RESER_R0/ RESER_R1/GXRP/RESER_R2/ RESER_R3	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF ((DA+FID) matches an entry in the learning table)), THEN use the Portmap in the learning table as the output ports. ELSE IF (DA matches an entry in the control table), THEN the output ports are the Portmap in the table. ELSE are the output ports are the intersection of the Pass Portmap (see 003D <sub>H</sub> <b>New Reserve Address Control Register 0</b> and 003E <sub>H</sub> <b>New Reserve Address Control Register 1</b> ) and the “Reserve Portmap” in the EEPROM (see 001C <sub>H</sub> , <b>RP</b> )
ARP/RARP	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF (ARP/RARP is trapped), THEN use ARP/RARP Portmap as the output ports. ELSE uses “Default Output Ports” as the output ports.

**Table 39 Forwarding Algorithm (cont'd)**

<b>Packets Identified by Samurai-6M/6MX (ADM6996M/MX)</b>	<b>Algorithm</b>
IGMP_IP/MLD_IP/MLD_IPV6	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE IF (Hardware IGMP Snooping is enabled), IF (Hardware IGMP Packet Ignore CPU Port is enabled), THEN forwards packets to Multicast Portmap but doesn't forward to the CPU port. Else forwards packets to Multicast Portmap. ELSE IF (IGMP_IP/MLD_IP/MLD_IPV6 is trapped), THEN use IGMP/IGMP_IP/MLD_IP/MLD_IPV6 Portmap as the output ports. ELSE uses "Default Output Ports" as the output ports.
TYPE	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE uses Type Portmap as the output ports.
PROTOCOL	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE uses Protocol Portmap as the output ports.
TCPUDP	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE uses TCPUDP Portmap as the output ports.
MAC_CTRL	IF (Portmap_Valid in the Special Tag is 1), THEN use Portmap in the Special Tag as the output ports. ELSE uses MAC CTRL Portmap as the output ports.
Others	Use "Default Output Ports" as the output ports

### 3.1.21 Special TAG

Special Tag is inserted after the Ethernet SA field allows the CPU to tell the switch how to handle the packets it sends or to know the source port when the CPU receives a packet.

8 Bytes	Preamble
6 Bytes	DA
6 Bytes	SA
Byte 0	Special Tag 0
Byte 1	Special Tag 1
Byte 2	Special Tag 2
Byte 3	Special Tag 3
Byte 4	Special Tag 4
Byte 5	Special Tag 5
4 Bytes	VLAN Tag
6 Bytes	SNAP
2 Bytes	Type/Length
	Data
4 Bytes	CRC

#### 3.1.21.1 Special Tag for the Receive

Users are allowed to enable Special TAG Receive (0011<sub>H</sub>, **STRE**) function to instruct Samurai-6M/6MX (ADM6996M/MX) to check the Special Tag to see if this field contains any commands when packets are received on the CPU port.

**Table 40 Special Tag for the Receive**

Special TAG	Description
Byte 0	ADM Prefix 0.
Byte 1	ADM Prefix 1. When Special TAG Receive is enabled, Samurai-6M/6MX (ADM6996M/MX) will compare {ADM Prefix -, ADM Prefix 1} with ADM TAG Ether Type (see 002E <sub>H</sub> , <b>ATET</b> ). If they are different, Special Tag is ignored. If they are the same, Samurai-6M/6MX (ADM6996M/MX) uses the Special Tag to make switching decisions.
Byte 2	Bit [7]: Don't care Bit [6]: Portmap_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [5:0]: Portmap in the Special Tag

**Table 40 Special Tag for the Receive (cont'd)**

Special TAG	Description
Byte 3	Bit [7]: Span_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [6]: Span 1 <sub>B</sub> Span packet 0 <sub>B</sub> Not span packet Bit [5]: Management_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [4]: Management 1 <sub>B</sub> Management packet 0 <sub>B</sub> Not management packet Bit [3]: Cross_VLAN_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [2]: Cross_VLAN 1 <sub>B</sub> Cross_Vlan packet 0 <sub>B</sub> Not Cross_VLAN packet Bit [1]: LRN_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [0]: LRN 1 <sub>B</sub> Learn 0 <sub>B</sub> Not Learn
Byte 4	Bit[7]: Ignore Bit[6]: PRI_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit[5:4]: PRI 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3 Bit [3]: Ignore Bit [2]: TXTAG_Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [1:0]: TXTAG
Byte 5	Bit [6]: Tagged Member Valid 1 <sub>B</sub> Valid 0 <sub>B</sub> Not Valid Bit [5:0]: Tagged Member, Bit[X] = 1: Port is in the tagged member

### 3.1.21.2 Special Tag for the Transmit

Users are allowed to enable Special TAG Transmit (0011<sub>H</sub>, **STTE**) function to instruct Samurai-6M/6MX (ADM6996M/MX) to insert the Special Tag followed SA in the packets transmitted from the CPU port. Samurai-6M/6MX (ADM6996M/MX) also allows users to choose what kinds of packets they don't want to insert this Special Tag even when Special TAG Transmit (0011<sub>H</sub>, **STTE**) function is enabled.

**Table 41 Option for Special Tag Transmit**

Packets Identified by Samurai-6M/6MX (ADM6996M/MX)	Condition	Result
BPDU/SLOW/PAE/RESER_R0/RESER_R1/GXRP/RESER_R2/RESER_R3	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert Reserve} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Reserve} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
ARP/RARP	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert ARP/RARP} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert ARP/RARP} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
IGMP_IP/MLD_IP/MLD_IPV6	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert Snoop} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Snoop} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
TYPE	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert Type} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Type} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
PROTOCOL	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert Protocol} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Protocol} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
TCPUDP	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert TCP/UDP} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert TCP/UDP} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
MAC_CTRL	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert MAC CTRL} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert MAC CTRL} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.

**Table 41 Option for Special Tag Transmit (cont'd)**

<b>Packets Identified by Samurai-6M/6MX (ADM6996M/MX)</b>	<b>Condition</b>	<b>Result</b>
Others	Special TAG Transmit = 0 <sub>B</sub> . or{Special TAG Transmit, Insert Default, Source Violation} = 100 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Default, Source Violation} = 110 <sub>B</sub> . or{Special TAG Transmit, Insert Default, Source Violation} = 101 <sub>B</sub> . {Special TAG Transmit, Insert Default, Source Violation} = 111 <sub>B</sub> .	Insert Special Tag

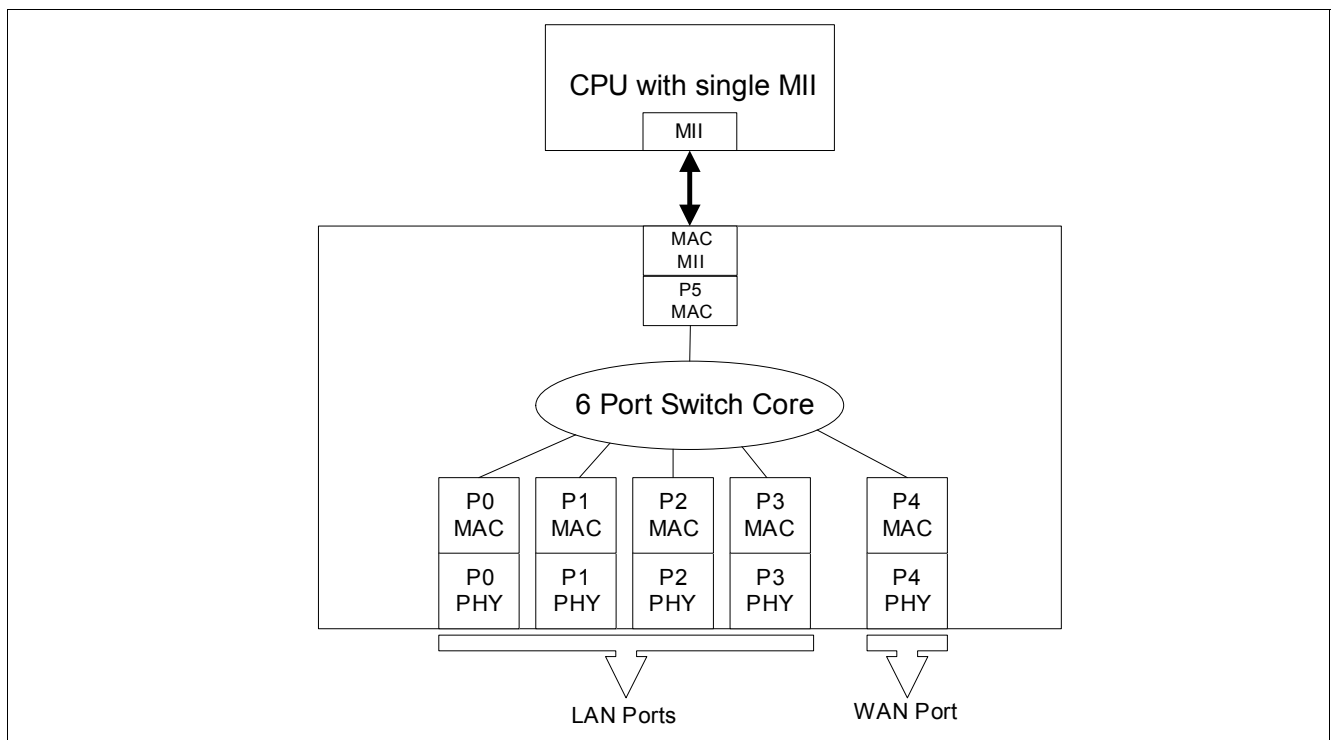
**Table 42 Special Tag for the Transmit**

<b>Special TAG</b>	<b>Description</b>
Byte 0	ADM Prefix 0.
Byte 1	ADM Prefix 1.
Byte 2	Bit [7]: Source Violation. 1 = This packet is a source violated packet and its forwarding algorithm to the CPU port was modified. 0 = This packet is not a source violated packet. Bit [6]: Mirror. 1 = This is a mirrored packet. 0 = This is not a mirrored packet. Bit [5]: Span. 1 = This is a span packet. 0 = This is not a span packet. Bit [4]: Management. 1 = This is a management packet. 0 = This is not a management packet. Bit [3]: Ignore. Bit [2:0]: Source Port. 000 <sub>B</sub> = Port 0. 001 <sub>B</sub> = Port 1. 010 <sub>B</sub> = Port 2. 011 <sub>B</sub> = Port 3. 100 <sub>B</sub> = Port 4. 101 <sub>B</sub> = Port 5.
Byte 3	Egress TAG[15:8].
Byte 4	Egress TAG[7:0].
Byte 5	Ignore.

### 3.2 Port4 and Port5 MII Connection

In ADM6996M/MX, there are 3 different configurations (Normal PHY, MAC type MII and PCS type MII, **CFG0**) for Port4. If Port4 is configured in normal PHY mode, then it is identical to Port0~Port3 and Port4's MII signals are ignored. If Port4 is configured in MAC type MII mode, it can be used for the HomePNA application and embedded single PHY will not be used. In ADM6996M/MX, the most popular is to configure Port4 as the PCS type MII for the router's WAN port application. Users can see **Figure 6** and **Figure 9** for more clear picture. For the Port5, there are three different configurations (MAC type MII mode, GPSI mode and RMII, **P5\_BUSMD0**) for connecting to CPU's MII/GPSI or RMII interface.

Here we depicted two general router applications of ADM6996M/MX, one is connected to CPU with single MII and another is connected to CPU with dual MII. In **Figure 6**, we can see either LAN to WAN or WAN to LAN, the packets will go through the same MII port. Because the CPU need to send out the packets with the registered MAC ID to the WAN port, and this MAC ID may also come in from the LAN ports. We know the switch learning scheme can't permit the packets with same MAC ID input from different ports. In the ADM6996M/MX design, we use the MAC clone and VLAN group to solve this problem. From **Figure 9**, users can have more details for this implementation.



**Figure 6 ADM6996M/MX to CPU with single MII Connection**

#### Implementation of WAN/LAN applications on Samurai

ADM6996M/MX implements WAN/LAN application by ADM6996M/MX Special TAG functions.

Special Tag is inserted after the Ethernet SA field to allow the CPU to tell the switch how to handle the packets it sends or to know the source port when the CPU receives a packet.

**Table 43 Special Tag**

Preamble	DA	SA	Special TAG 0	Special TAG 1	Special TAG 2	Special TAG 3	Special TAG 4	Special TAG 5	VLAN Tag	SNAP	Type/Length	Data	CRC
8B	6B	6B	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	4B	6B	2B		4B



Step 1: Set EEPROM 11<sub>H</sub>[12]=1 to enable Special TAG Receive (CPU to ADM6996M/MX).  
 Step 2: Set EEPROM 11<sub>H</sub>[11]=1 to enable Special TAG Transmit (ADM6996M/MX to CPU).  
 Set EEPROM 11<sub>H</sub>[15:13] to assign CPU Port Number. Default CPU Port is "101 - Port5".  
 Set EEPROM 0B<sub>H</sub>[5] to set the option whether ADM6996M/MX CPU Port checks CRC for the packet with Special TAG Receive.  
 Set EEPROM 11<sub>H</sub>[10] to set the option whether ADM6996M/MX adds Special TAG Transmit to Pause frame.  
 The configurations are as follows.

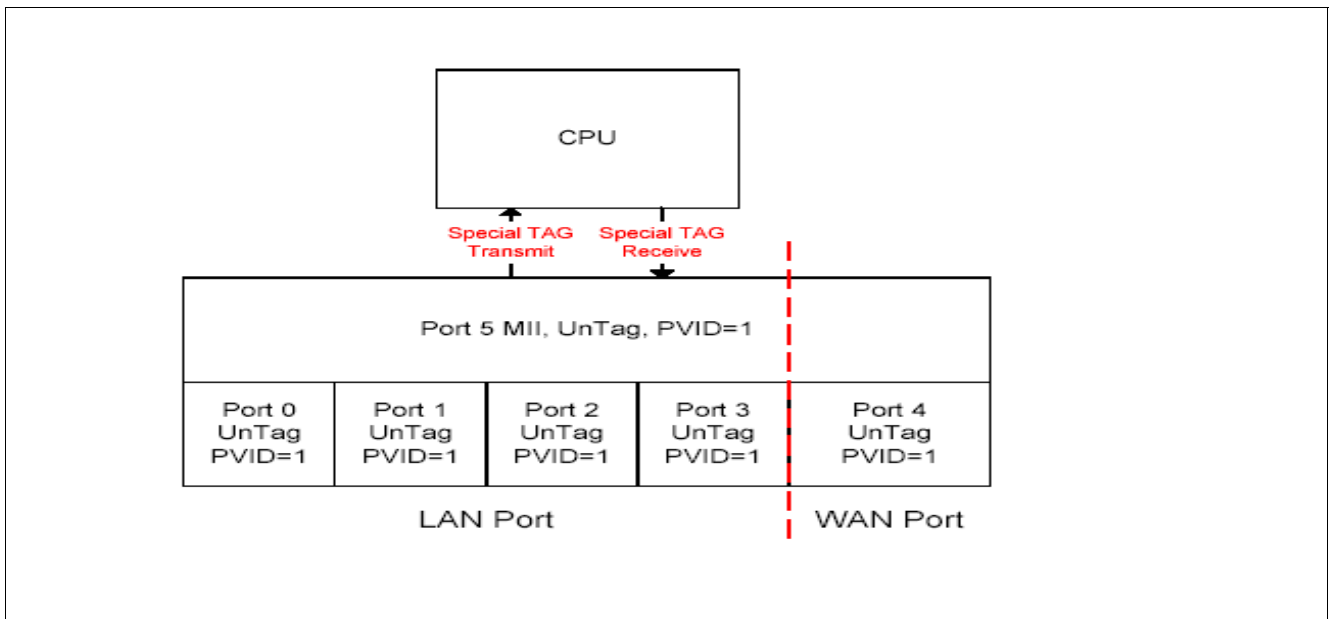


Figure 7 The configurations of the implementation by ADM6996M/MX Special TAG functions

- Step 1: Set ADM6996M/MX to port-based VLAN mode (default)
- Step 2: Set WAN/LAN group

Table 44 Set WAN/LAN Group

EEPROM	Received Port	Forwarding Group					
	Port-based Group	Port 0	Port 1	Port 2	Port 3	Port 4	Port 5
40 <sub>H</sub>	Port 0	✓	○	○	○		✓
42 <sub>H</sub>	Port 1	○	✓	○	○		✓
44 <sub>H</sub>	Port 2	○	○	✓	○		✓
46 <sub>H</sub>	Port 3	○	○	○	✓		✓
48 <sub>H</sub>	Port 4(WAN Port)					✓	✓
4A <sub>H</sub>	Port 5(CPU Port)	✓	✓	✓	✓	✓	✓

Note: "✓" is necessary and "○" is option to implement Port-based VLAN function of LAN group.

Port 0, Port 0/1/2/3/5, set REG 40<sub>H</sub> to 002F<sub>H</sub>  
 Port 1, Port 0/1/2/3/5, set REG 42<sub>H</sub> to 002F<sub>H</sub>  
 Port 2, Port 0/1/2/3/5, set REG 44<sub>H</sub> to 002F<sub>H</sub>  
 Port 3, Port 0/1/2/3/5, set REG 46<sub>H</sub> to 002F<sub>H</sub>  
 Port 4, Port 4/5, set REG 48<sub>H</sub> to 0030<sub>H</sub>  
 Port 5, Port 0/1/2/3/4/5, set REG 4A<sub>H</sub> to 003F<sub>H</sub>

- Step 3: Set EEPROM 11<sub>H</sub>[12:11]="11" to enable Special TAG Receive/Transmit Enable

Software Operation:

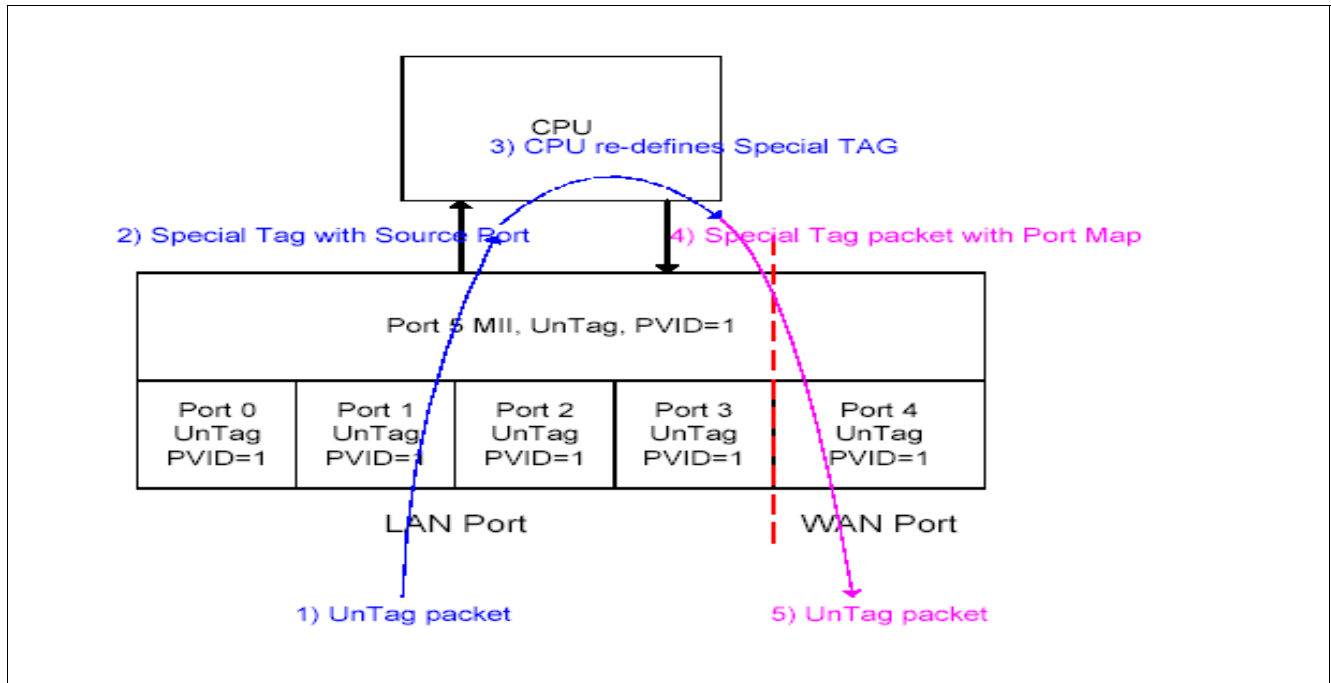


Figure 8 Software Operation

- Step 1:
  - If Untag packet received from LAN Port forwards to CPU Port, ADM6996M/MX will insert Special TAG followed SA in the packets transmitted from the CPU port. ADM6996M/MX also allows users to choose what kinds of packets they don't want to insert this Special TAG in.

Table 45 Packets Identified by ADM6996M/MX

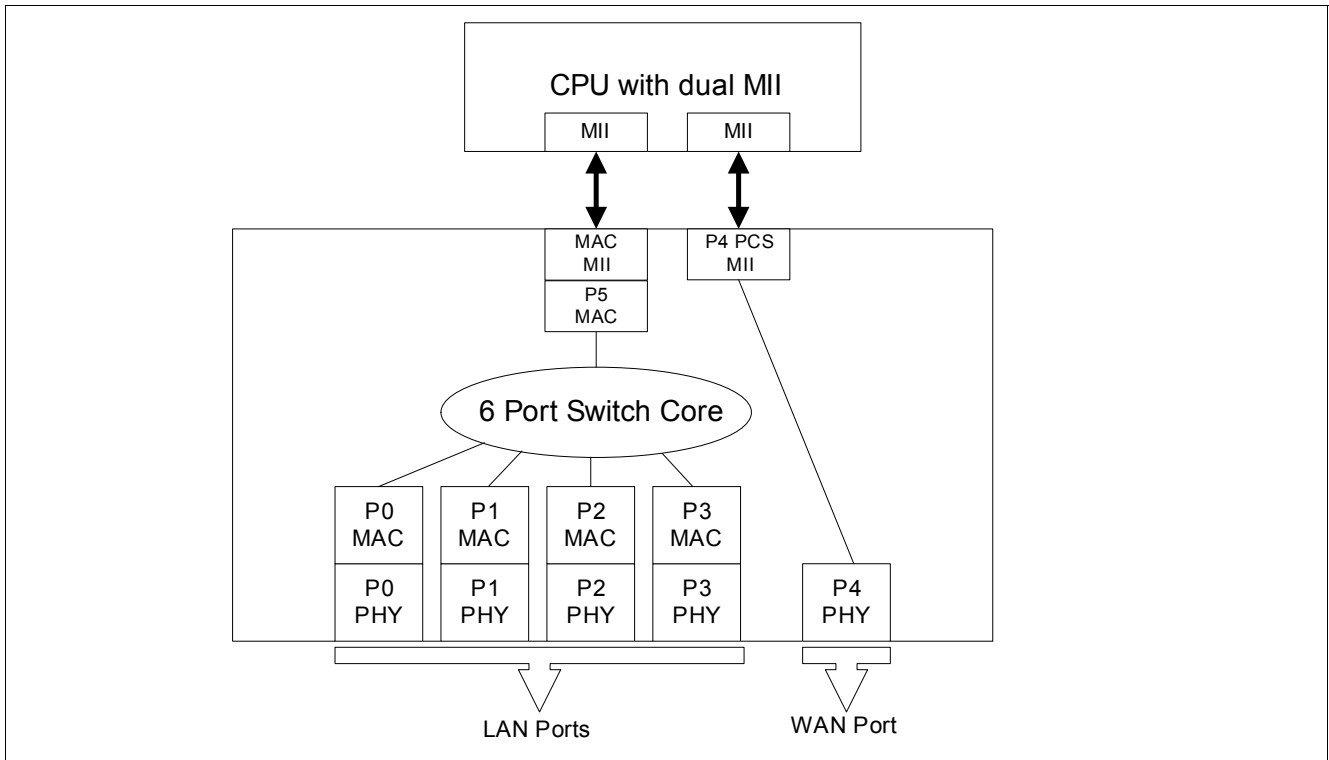
Packets Identified by ADM6996M/MX	Condition (EEPROM 0x11h[11] and 0x99h[8:0])	Result
BPDU/SLOW/ PAE/RESER_R0/ RESER_R1/ GXR/PAE/ RESER_R2/ RESER_R3	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert Reserve} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Reserve} = 11 <sub>B</sub>	Insert Special Tag on the CPU port.
ARP/RARP	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert ARP/RARP} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert ARP/RARP} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
IGMP_IP/MLD_IP/ MLD_IPV6	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert Snoop} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Snoop} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.

**Table 45 Packets Identified by ADM6996M/MX (cont'd)**

Packets Identified by ADM6996M/MX	Condition (EEPROM 0x11h[11] and 0x99h[8:0])	Result
TYPE	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert Type} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Type} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
PROTOCOL	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert Protocol} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Protocol} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
TCPUDP	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert TCP/UDP} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert TCP/UDP} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
MAC_CTRL	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert MAC CTRL} = 10 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert MAC CTRL} = 11 <sub>B</sub> .	Insert Special Tag on the CPU port.
Others	Special TAG Transmit = 0 <sub>B</sub> . or {Special TAG Transmit, Insert Default, Source Violation} = 100 <sub>B</sub> .	Don't insert Special Tag on the CPU port.
	{Special TAG Transmit, Insert Default, Source Violation} = 110 <sub>B</sub> . or {Special TAG Transmit, Insert Default, Source Violation} = 101 <sub>B</sub> .	Insert Special Tag
	{Special TAG Transmit, Insert Default, Source Violation} = 111 <sub>B</sub> .	

- Step 2: CPU must re-define the Special TAG for the Receive to determine the destination group.
- Step 3: If **MAC\_CLONE** function is enabled, CPU must set **LRN** parameter to disable learning mechanism for specific packet.

In **Figure 9**, it shows an easy way to connect the CPU with dual MII for the routing application. In this application, Port4's embedded and isolated PHY will be connected to the WAN port. CPU will act as the bridge to translate the packet's frame for LAN/WAN and use different MII to handle the packets either from LAN to WAN or from WAN to LAN. The isolated PHY is helpful to reduce the BOM cost.

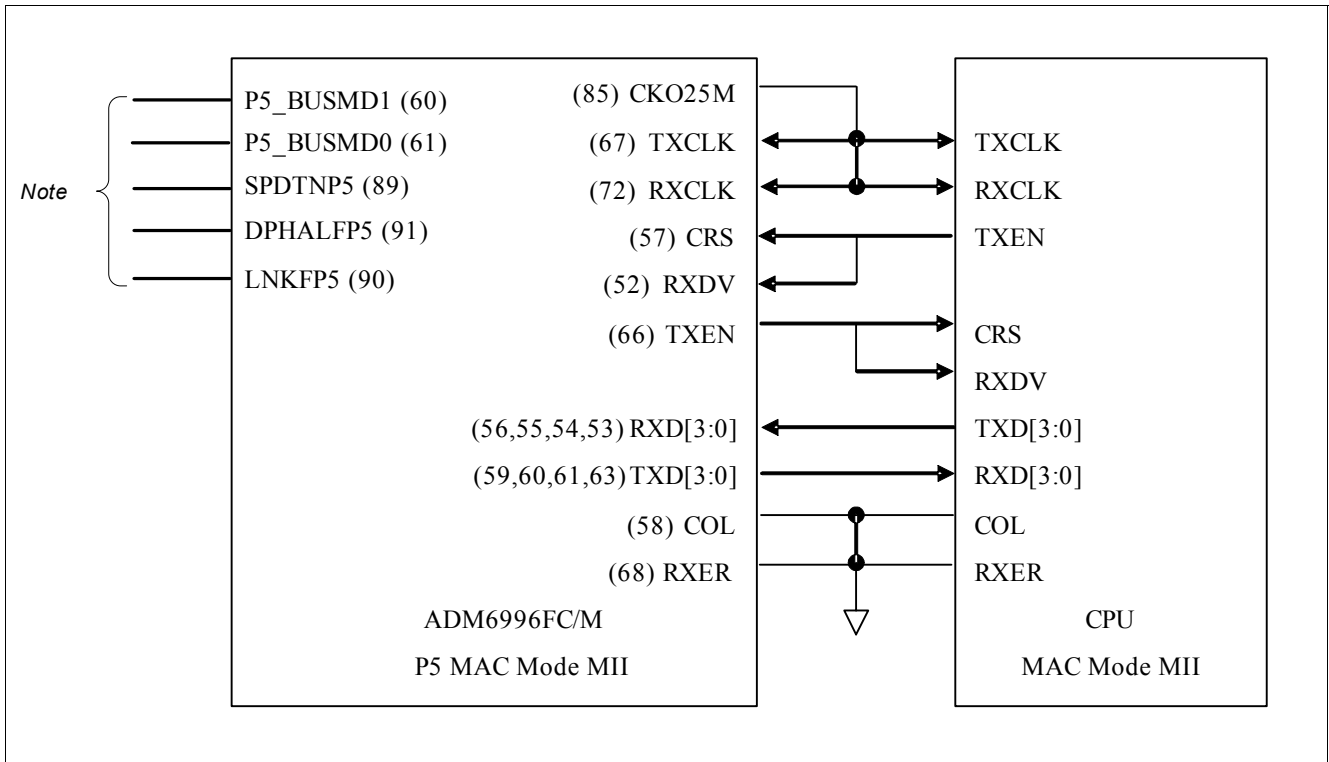


**Figure 9 ADM6996M/MX to CPU with dual MII Connection**

Normally, the MAC mode MII should be connected to the PHY mode MII. But in some applications, we need to connect both MAC mode MII to each other as shown. In [Figure 9](#), due to most CPU's MII being MAC mode, Port4 is PCS to MAC connection and Port5 is MAC to MAC connection.

Through the hardware setting, it is easy to set ADM6996M/MX Port5 MII to be operating in 100M Full duplex mode. And this kind mode (100M Full) is normally the operation mode to be with CPU, the interface connection is described in the following diagram.

- (1) CKO25M is the 25M clock driven out by ADM6996M/MX to fit 100M MII operation. This clock output provides 8mA driving capability and it can directly connected to TXCLK/RXCLK.
- (2) Due to Full duplex mode, so COL is tied to GND.

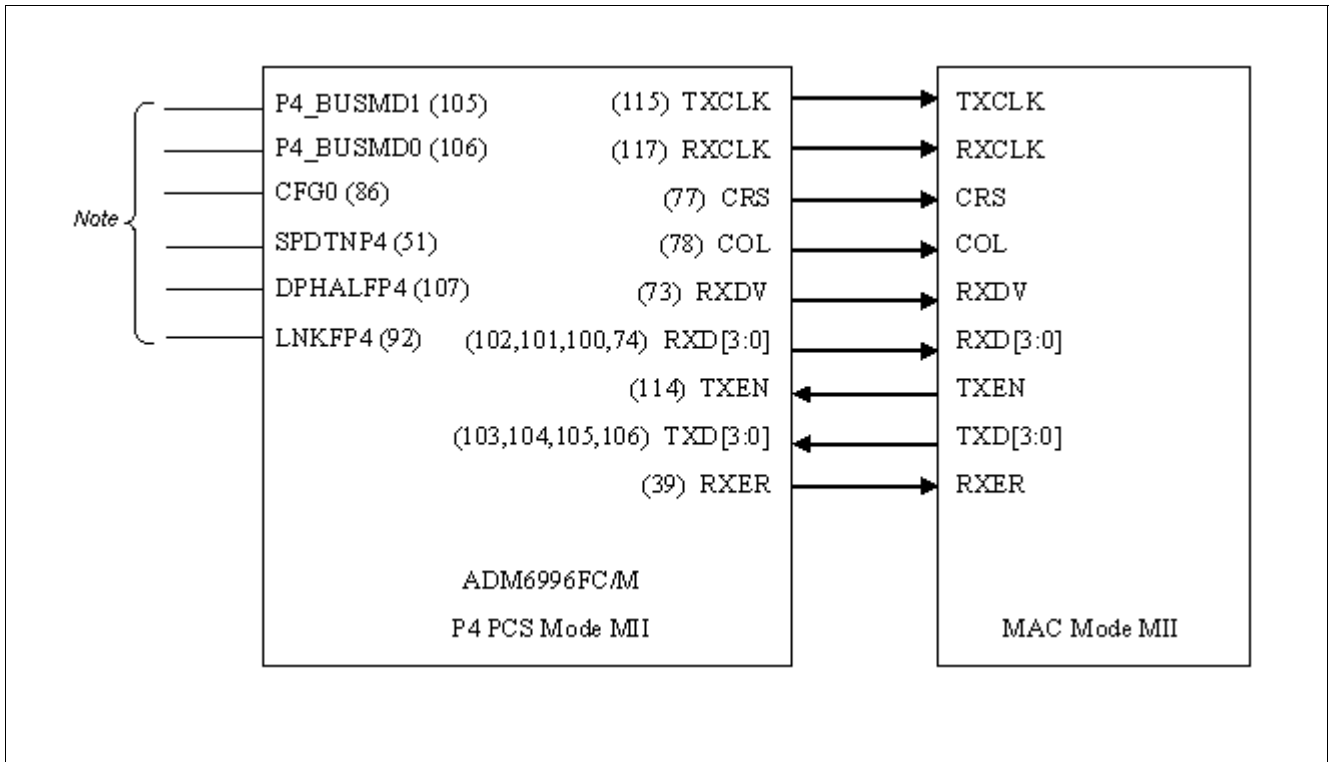


**Figure 10 100M Full duplex MAC to MAC MII Connection**

Note:

1. Pin 60 and pin 61 should be pull low to let P5\_BUSMD be latched as "00" and make Port5 be operating in MII mode (**P5\_BUSMD0**).
2. Pin 89 (SPDTNP5) should be pull low or floating to set Port5 be operating in 100Mbit/s.
3. Pin 91 (DPHALFP5) should be pull low or floating to set Port5 be operating in full duplex mode.
4. Pin 90 (LNKFP5) should be pull low or floating to set Port5 Link up.

About the PCS mode MII connecting to MAC mode MII, it's very straightforward. If PCS and MAC follow the MII standard timing and users notice the PCB layout balance, it should not be an issue for PCS to connect to the MAC. In [Figure 11](#), we depicted this interface connection and described how to configure Port4 as the PCS mode MII.



**Figure 11 PCS to MAC MII connection**

Note:

5. From the **CFG0** pin description, we know it needs to set {CFG0, P4\_BUSMD[1:0]} as 1xx<sub>B</sub> to configure Port4 be operating in PCS mode MII. So it doesn't matter the value on P4\_BUSMD[1:0] (pin 105 and pin 106) and we only pull high the CFG0 or make it floating (due to it has internally pull high) is ok.
6. Pin 51 (SPDTNP4) acts as DUPLEX LED for Port 4; in half duplex mode, it is collision LED for each port.
7. Pin 107 (DPHALFP4) used to indicate the speed status of Port 4.
8. Pin 92 (LNKFP4) used to indicate the link/activity status of Port 4.

### 3.3 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- 100Base-X physical medium dependent (PMD)

The 10Base-T section of the device implements the following functional blocks:

- 10Base-T physical layer signaling (PLS)
- 10Base-T physical medium attachment (PMA)

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface.

Auto MDIX function is supported. This function can be Enable/Disabled by the hardware pin.

The Digital approach for the integrated PHY of Samurai-6M/6MX (ADM6996M/MX) has been adopted.

### 3.3.1 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further details regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The Samurai-6M/6MX (ADM6996M/MX) supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the Samurai-6M/6MX (ADM6996M/MX) can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software enables bit 12 in MII register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the Samurai-6M/6MX (ADM6996M/MX) transmits the abilities programmed into the auto negotiation advertisement register at address 04h via FLP bursts. Any combination of 10 Mbit/s, 100 Mbit/s, half duplex, and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05<sub>H</sub>.

The contents of the “auto negotiation link partner ability register” are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04<sub>H</sub> and 05<sub>H</sub> and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

100Base-TX full duplex (highest priority)

100Base-TX half duplex

10Base-T full duplex

10Base-T half duplex (lowest priority)

The basic mode control register at address 0h provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbit/s or 100 Mbit/s operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register at address 1h indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the Samurai-6M/6MX (ADM6996M/MX). The BMSR also provides status on:

Whether auto negotiation is complete (bit 5)

Whether the Link Partner is advertising that a remote fault has occurred (bit 4)

Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4h indicates the auto negotiation abilities to be advertised by the Samurai-6M/6MX (ADM6996M/MX). All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05h indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bit (bit 5, register address 1h) is set.

### 3.3.2 Speed/Duplex Configuration

The twelve sets of four pins listed in [Table 46](#) configure the speed/duplex capability of each channel of Samurai-6M/6MX (ADM6996M/MX). The logic states of these pins are latched into the advertisement register (register

address 4<sub>H</sub>) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0<sub>H</sub>) according to [Table 46](#).

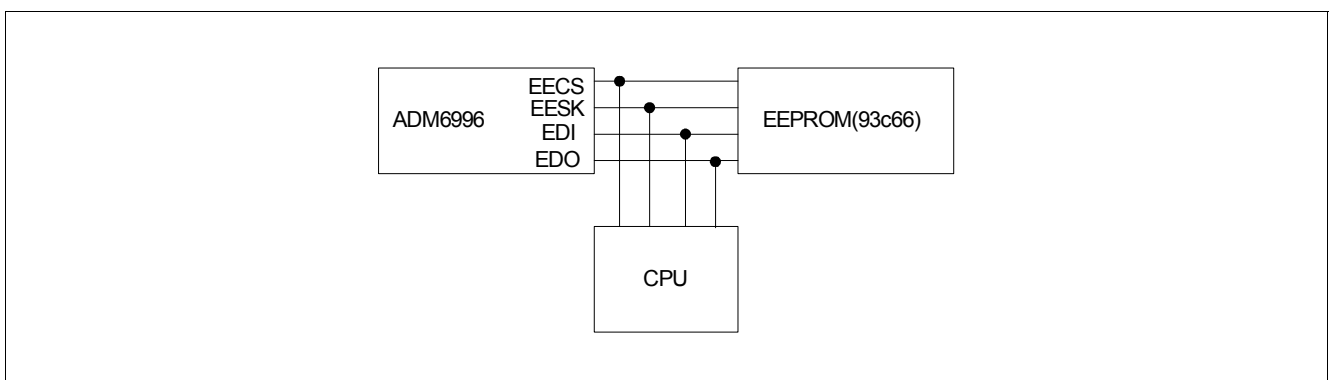
In order to make these pins have the same Read/Write priority as software, they should be programmed to 11111111b in case user likes to update the advertisement register through software.

**Table 46 Speed/Duplex Configuration**

Auto Negotiation (Pin & EEPROM)	Speed (Pin & EEPROM)	Duplex (Pin & EEPROM)	Auto Negotiation	Advertise Capability				Parallel Detect Capability			
				100F	100H	10F	10H	100F	100H	10F	10H
1	1	1	1	1	1	1	1	0	1	0	1
1	1	0	1	0	1	0	1	0	1	0	1
1	0	1	1	0	0	1	1	0	0	0	1
1	0	0	1	0	0	0	1	0	0	0	1
0	1	1	0	1	—	—	—	—	—	—	—
0	1	0	0	—	1	—	—	—	—	—	—
0	0	1	0	—	—	1	—	—	—	—	—
0	0	0	0	—	—	—	1	—	—	—	—

### 3.4 Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the Samurai-6M/6MX (ADM6996M/MX): (1) Hardware Setting (2) EEPROM Interface (3) SMI Interface. Users can use the EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See [Figure 12](#) for the description.



**Figure 12 Interconnection between Samurai-6M/6MX (ADM6996M/MX), EEPROM and CPU**

#### 3.4.1 Hardware Setting

The Samurai-6M/6MX (ADM6996M/MX) provides some hardware pins, where values residing on will be strapped for the default setting during the power on or reset.



**Table 47 Hardware Setting**

Setting Name	Description
<b>GFCEN</b>	Global Flow Control Enable. 0 <sub>B</sub> Flow Control Capability is depended upon the register setting in corresponding EEPROM register 1 <sub>B</sub> All ports flow control capability is enabled.
<b>SDIO_MD</b>	SDC/SDIO mode selection. 0 <sub>B</sub> 16 bits mode
P5_BUSMD[1:0]	Port 5 bus mode selection bit 0. P5_BUSMD[1:0] ,Interface 00 <sub>B</sub> MII 01 <sub>B</sub> GPSI 10 <sub>B</sub> RMII 11 <sub>B</sub> Reserved and Not Allowed.
{CFG0, P4_BUSMD[1:0]}	Bus Mode of Port 4 0_00 <sub>B</sub> PHY Interface 0_01 <sub>B</sub> MAC MII 1_XX <sub>B</sub> PCS MII
<b>BPEN</b>	Recommend Back-Pressure in half-duplex. 0 <sub>B</sub> Disable Back-Pressure. 1 <sub>B</sub> Enable Back-Pressure
<b>RECANEN</b>	Recommend Auto Negotiation Enable. Only valid for Twisted pair interface. Programmed this bit to 1 has no effect to Fiber port. 0 <sub>B</sub> Disable all TP port auto negotiation capability 1 <sub>B</sub> Enable all TP port auto negotiation capability
<b>XOVEN</b>	Cross Over Enable. Only available in TP interface. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
<b>LED_MODE</b>	Enable Mac to choose LED Display Mode. 0 <sub>B</sub> Single color LED 1 <sub>B</sub> Dual color LED

### 3.4.2 EEPROM Interface

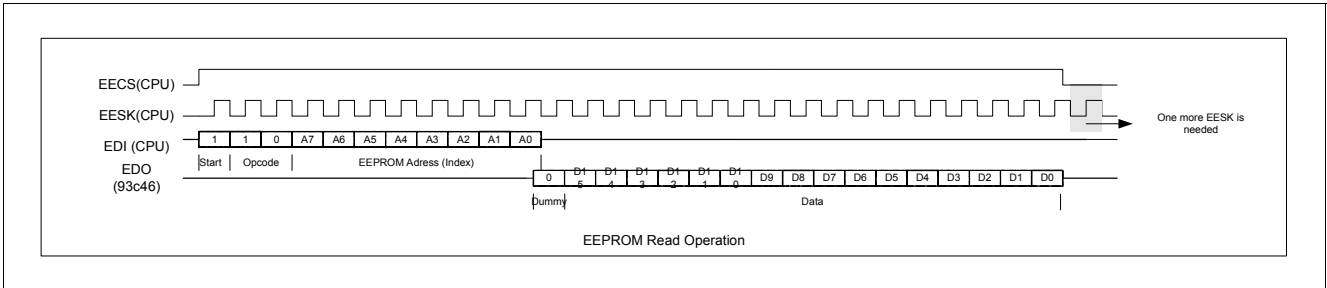
The EEPROM Interface is provided to easily configure the setting without the CPU's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the Samurai-6M/6MX (ADM6996M/MX) will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = 4154<sub>H</sub>, it will load all the data in the 93c66. If not, the Samurai-6M/6MX (ADM6996M/MX) will stop loading the 93c66. The user also can pull down the **EDO** to force the Samurai-6M/6MX (ADM6996M/MX) not to load the 93c66. The 93c66 loading time is around 30ms. Then CPU should drive the high-z value in the **EECS**, **EESK** and **EDI** pins in this period if existing the CPU to read or write the registers in the Samurai-6M/6MX (ADM6996M/MX).

The EEPROM Interface needs only one Write command to complete a "Write" operation to the Samurai-6M/6MX (ADM6996M/MX). If users would like to update the 93c66 at the same time, then three commands, Write Enable, Write, and Write Disable, are needed to complete this operation (See 93c66 Spec. for the reference). Users should note that the EEPROM interface only allows the CPU to write the EEPROM register in the Samurai-6M/6MX

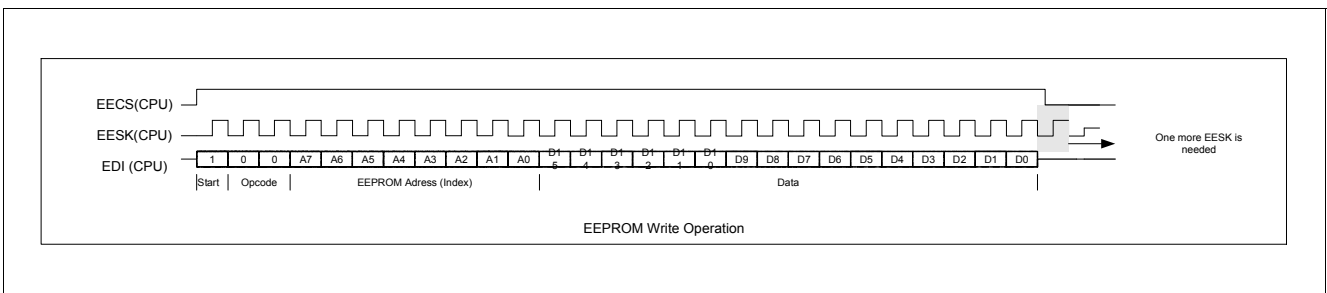
**Function Description**

(ADM6996M/MX) and doesn't support the READ command. If the CPU sends out the Read Command, then 93c66 will respond with the value inside, instead of Samurai-6M/6MX (ADM6996M/MX). Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write).

(1) Read 93c66 via the EEPROM Interface (Index = 2, Data = 1111<sub>H</sub>).

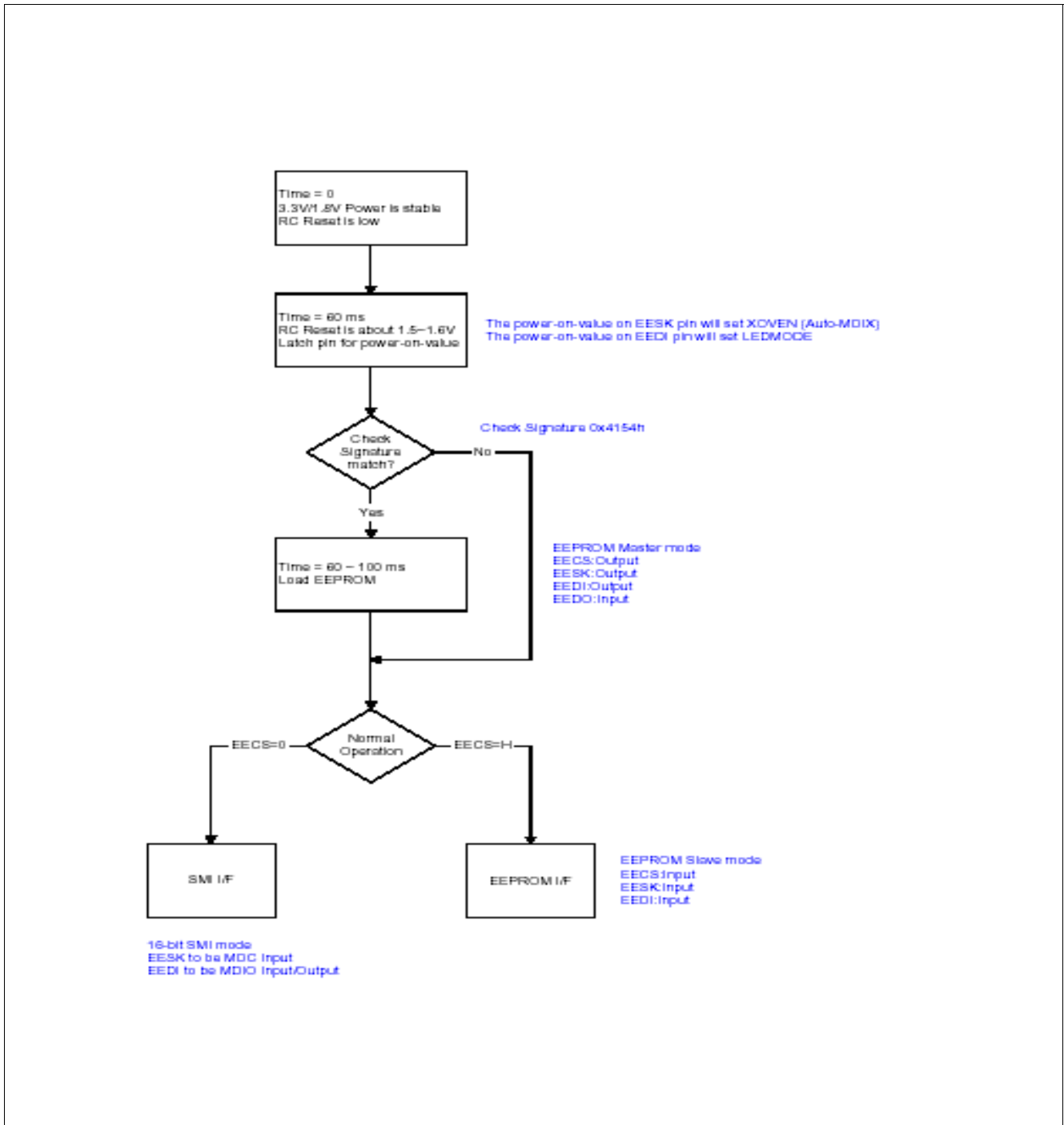


(2) Write EEPROM registers in the Samurai-6M/6MX (ADM6996M/MX) (Index = 2, Data = 16'h2222).



**Power-On-Sequence of Samurai**

The following diagram shows the power-on-sequence of Samurai.



**Figure 13 The Power-On-Sequence of Samurai**

Set ADM6996LC/FC Pin59 SDIO\_MD=1 to 16-bit SMI mode.

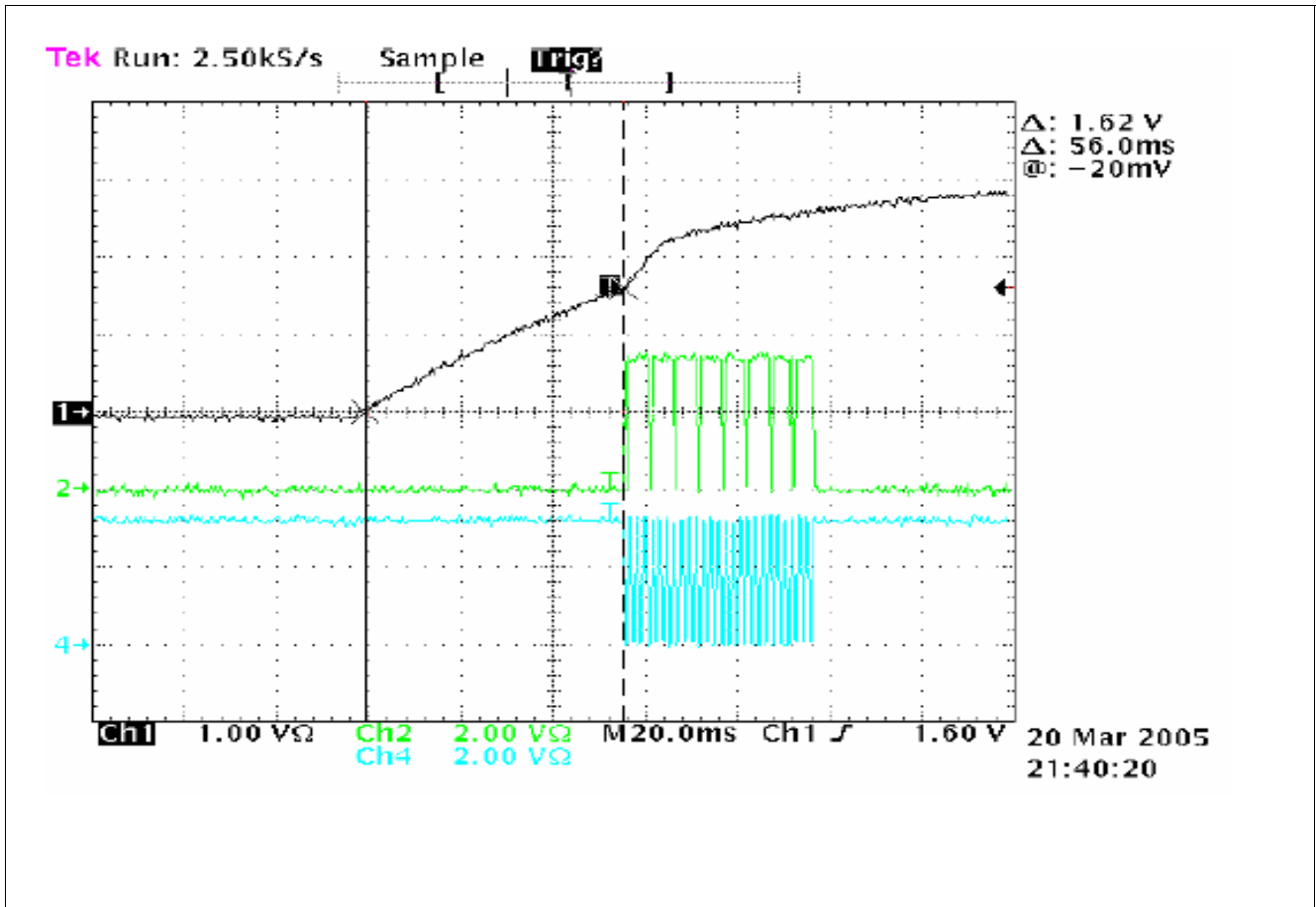
Set ADM6996I/M Pin59 SDIO\_MD=0(default) to 16-bit SMI mode.

Timing Diagram of RC, EECS and EESK (with correct signature EEPROM)

Waveform 1: RC Reset

Waveform 2: EECS

Waveform 4: EESK



**Figure 14 Timing Diagram of RC, EECS and EESK (with correct signature EEPROM)**

Timing Diagram of RC, EECS and EESK (without EEPROM)

Waveform 1: RC Reset

Waveform 2: EECS

Waveform 4: EESK

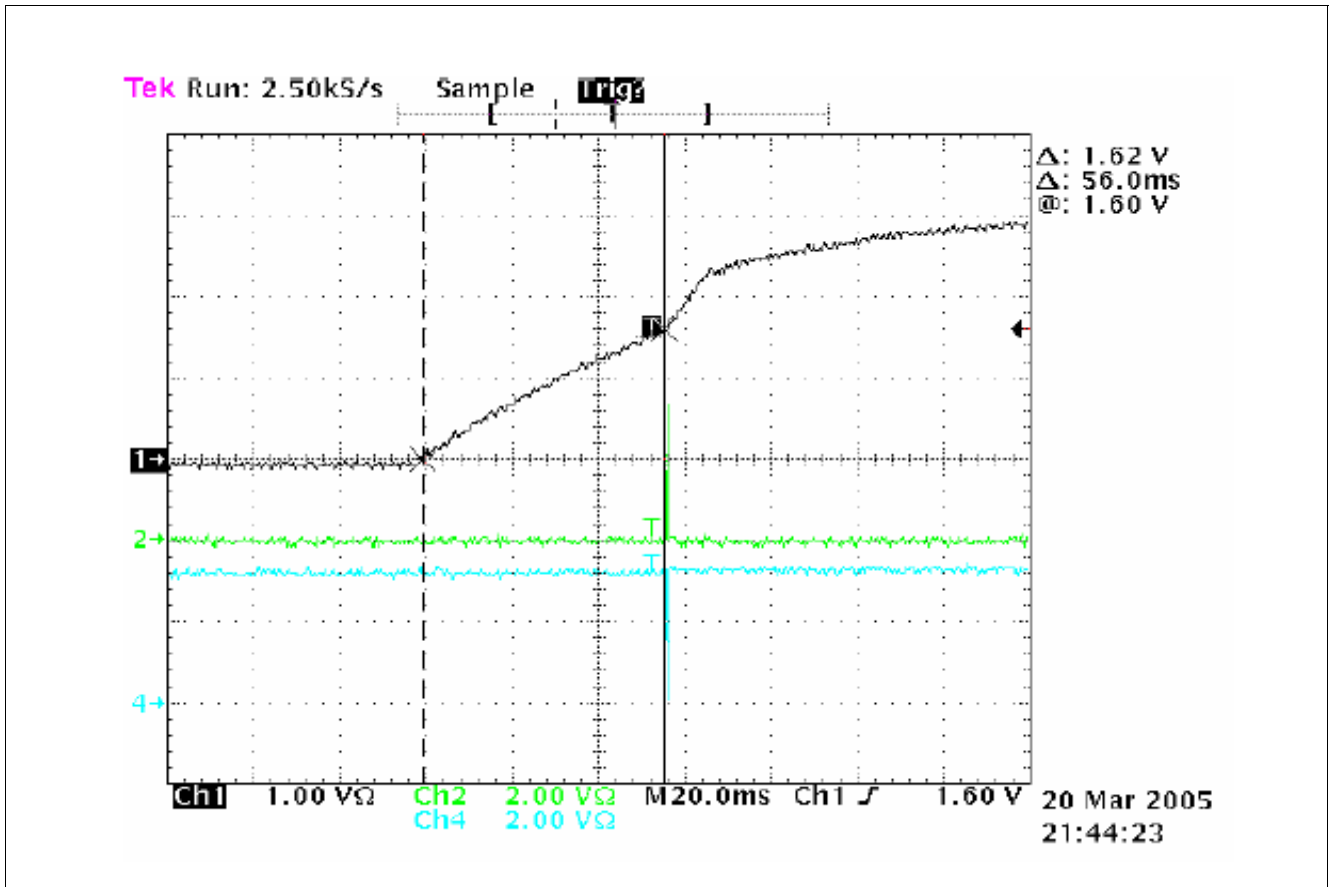


Figure 15 Timing Diagram of RC, EECS and EESK (without EEPROM)

### 3.4.3 SMI Interface

The SMI consists of two pins, management data clock (**EESK**) and management data input/output (**EDI**). The Samurai-6M/6MX (ADM6996M/MX) is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin is needed to pull low if EEPROM interface is also used.

The EDI pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. Samurai-6M/6MX (ADM6996M/MX) requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a <01<sub>B</sub>> pattern. The next field signals the operation code (OP): <10<sub>B</sub>> indicates read from management register operation, and <01<sub>B</sub>> indicates write to management register operation. The next field is the management register address. It is 10 bits wide and the most significant bit is transferred first.

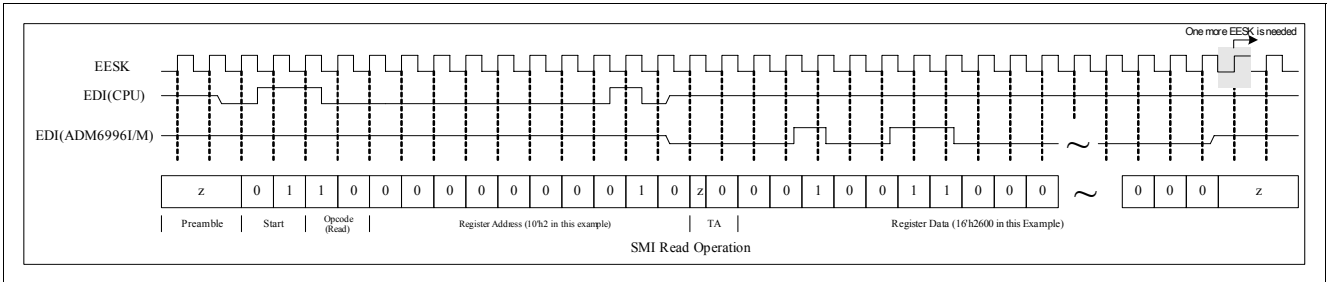
During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the management registers of the Samurai-6M/6MX (ADM6996M/MX).

#### (A) Preamble Suppression

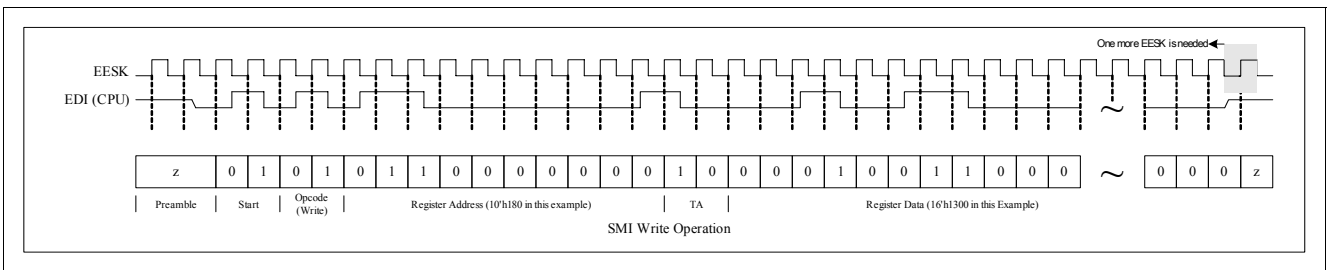
The SMI of Samurai-6M/6MX (ADM6996M/MX) supports a preamble suppression mode. The Samurai-6M/6MX (ADM6996M/MX) requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI. While the Samurai-6M/6MX (ADM6996M/MX) will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When Samurai-6M/6MX (ADM6996M/MX) detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then Samurai-6M/6MX (ADM6996M/MX) will tristate the EDI pin.

**(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 16'h2600)**



**(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 16'h1300)**

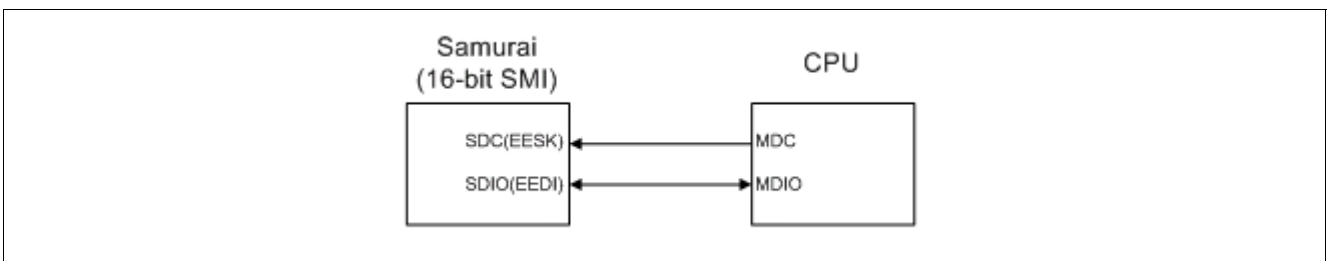


**Table 48 (D) The Pin Type of EECS, EESK, EDI and EDO during the Operation**

Pin Name	Reset Operation	Load EEPROM	Write Operation	Read Operation
EECS	Input	Output	Input	Input
EESK	Input	Output	Input	Input
EDI	Input	Output	Input	Input/Output
EDO	Input	Input	Input	Input

**How to Use Samurai 16-bit Mode SMI to Access EEPROM/Counter/PHY Register by CPU MDC/MDIO Interface**

Samurai supports 16-bit mode SMI interface to access EEPROM/Counter/PHY Register by CPU MDC/MDIO interface. The SMI interface consists of two pins, management data clock (EESK) and management data input/output (EEDI).



**Figure 16 SMI Interface**

- The difference between SMI Command and MDC/MDIO Command
  - Samurai SMI Command uses 10-bit register address to access allocate EEPROM/Counter/PHY Register.

**Memory Map**

**Table 49 Memory Map**

Register	Definition
0000 <sub>H</sub> ~ 003F <sub>H</sub>	EEPROM BAISC Register Map
0040 <sub>H</sub> ~ 009B <sub>H</sub>	EEPROM Extended Register Map
00A0 <sub>H</sub> ~ 0143 <sub>H</sub>	Counter and Switch Status Map
0200 <sub>H</sub> ~ 02FF <sub>H</sub>	PHY Register Map

So you need to divide 10-bit register address to 5-bit PHY address and 5-bit REG address of MDC/MDIO command to access EEPROM/Counter Register Map. For Samurai PHY Register Map, you can set the 5-bit PHY address = '10000' and use the standard REG address to access P0~P4 PHY MII Register.

**3.5 The Hardware Difference between ADM6996M/MX and ADM6996F**

ADM6996FC is a power-down version to replace ADM6996F and ADM6996M/MX is advanced function version for new applications.

**Pin Description(QFP128)**

**Table 50 Pin Description(QFP128)**

Pin No.	ADM6996M/MX	ADM6996F	Notes
59	P5TXD3(SDIO_MD)	P5TXD3(VOL23)	For ADM6996FC, SDIO_MD=0 default 32bit mode For ADM6996M/MX, SDIO_MD=0 default 16bit mode Add pull-up/down resistor for ADM6996F/FC/M compatible design to avoid wrong power-on-latch.
60	P5TXD2(RMIISEL)	P5TXD2(ROMCODE25 )	Add pull down resistor for ADM6996F/FC/M P5 MII mode to avoid wrong power-on-latch.
61	P5TXD1(7WIRE)	P5TXD1(P5GPSI)	Add pull down resistor for ADM6996F/FC/M P5 MII mode to avoid wrong power-on-latch.
65	INT_N	VCCIK(1.8V Digital)	Interrupt for Learning Table Access/Port Security/Counter Overflow/Port Status Add a option design to CPU INT_N pin

## 4 Registers Description

The EEPROM provides Samurai-6M/6MX (ADM6996M/MX) with many option settings

### Main Settings

- Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.
- VLAN & TOS Priority Mapping
- Broadcast Storming rate and Trunk.
- Fiber Select, Auto MDIX select
- VLAN Mapping
- Per Port Buffer number

**Table 51 Registers Address Space**

Module	Base Address	End Address	Note
EEPROM Basic Register Map	0000 <sub>H</sub>	003F <sub>H</sub>	
EEPROM Extended Register Map	0040 <sub>H</sub>	009C <sub>H</sub>	
Counter and Switch Status Map	00A0 <sub>H</sub>	0143 <sub>H</sub>	
PHY Register Map	0200 <sub>H</sub>	02FF <sub>H</sub>	

**Table 52 Registers Overview**

Register Short Name	Register Long Name	Offset Address	Page Number
<b>SIG</b>	Signature Register	00 <sub>H</sub>	<b>90</b>
<b>P0BC</b>	P0 Basic Control Register	01 <sub>H</sub>	<b>90</b>
<b>P0EC</b>	P0 Extended Control Register	02 <sub>H</sub>	<b>92</b>
<b>P1EC</b>	P1 Extended Control Register	02 <sub>H</sub>	<b>93</b>
<b>P1BC</b>	P1 Basic Control Register	03 <sub>H</sub>	<b>92</b>
<b>P2EC</b>	P2 Extended Control Register	04 <sub>H</sub>	<b>93</b>
<b>P3EC</b>	P3 Extended Control Register	04 <sub>H</sub>	<b>93</b>
<b>P2BC</b>	P2 Basic Control Register	05 <sub>H</sub>	<b>92</b>
<b>P4EC</b>	P4 Extended Control Register	06 <sub>H</sub>	<b>93</b>
<b>P5EC</b>	P5 Extended Control Register	06 <sub>H</sub>	<b>93</b>
<b>P3BC</b>	P3 Basic Control Register	07 <sub>H</sub>	<b>92</b>
<b>P4BC</b>	P4 Basic Control Register	08 <sub>H</sub>	<b>92</b>
<b>P5BC</b>	P5 Basic Control Register	09 <sub>H</sub>	<b>92</b>
<b>SC0</b>	System Control Register 0	0A <sub>H</sub>	<b>93</b>
<b>SC1</b>	System Control Register 1	0B <sub>H</sub>	<b>94</b>
<b>MS</b>	Multicast Snooping Register	0C <sub>H</sub>	<b>96</b>
<b>AR</b>	ARP/RARP Register	0D <sub>H</sub>	<b>99</b>
<b>VPM</b>	VLAN Priority Map Register	0E <sub>H</sub>	<b>100</b>
<b>TPM</b>	TOS Priority Map Register	0F <sub>H</sub>	<b>101</b>
<b>SC2</b>	System Control Register 2	10 <sub>H</sub>	<b>102</b>
<b>SC3</b>	System Control Register 3	11 <sub>H</sub>	<b>103</b>



**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<b>SC4</b>	System Control Register 4	12 <sub>H</sub>	<b>104</b>
<b>P0SO</b>	Port 0 Security Option	13 <sub>H</sub>	<b>106</b>
<b>P1SO</b>	Port 1 Security Option	14 <sub>H</sub>	<b>107</b>
<b>P2SO</b>	Port 2 Security Option	15 <sub>H</sub>	<b>107</b>
<b>P3SO</b>	Port 3 Security Option	16 <sub>H</sub>	<b>107</b>
<b>P4SO</b>	Port 4 Security Option	17 <sub>H</sub>	<b>107</b>
<b>P5SO</b>	Port 5 Security Option	18 <sub>H</sub>	<b>107</b>
<b>UFGPM</b>	Unicast Port Map and Forward Group Port Map	19 <sub>H</sub>	<b>108</b>
<b>BFGPM</b>	Broadcast Port Map and Forward Group Port Map	1A <sub>H</sub>	<b>108</b>
<b>MFGPM</b>	Multicast Port Map and Forward Group Port Map	1B <sub>H</sub>	<b>109</b>
<b>RFGPM</b>	Reserve Port Map and Forward Group Port Map	1C <sub>H</sub>	<b>110</b>
<b>PIOFGPM</b>	Packet Identification Option, Forward Group Port Map	1D <sub>H</sub>	<b>111</b>
<b>VPEFGPM</b>	VLAN Priority Enable and Forward Group Port Map	1E <sub>H</sub>	<b>112</b>
<b>SPEFGPM</b>	Service Priority Enable and Forward Group Port Map	1F <sub>H</sub>	<b>113</b>
<b>IFNTFGPM</b>	Input Force No Tag and Forward Group Port Map	20 <sub>H</sub>	<b>114</b>
<b>IFFGPM</b>	Ingress Filter and Forward Group Port Map	21 <sub>H</sub>	<b>115</b>
<b>VSDFGPM</b>	VLAN Security Disable and Forward Group Port Map	22 <sub>H</sub>	<b>116</b>
<b>BT0</b>	Buffer Threshold Register 0	23 <sub>H</sub>	<b>118</b>
<b>BT1</b>	Buffer Threshold Register 1	24 <sub>H</sub>	<b>118</b>
<b>IMEIJT</b>	IGMP/MLDTRAP Enable and Input Jam Threshold Register	25 <sub>H</sub>	<b>118</b>
<b>Q2WVECPO</b>	Queue 2 Weight, VID Exist Check, and PPPOE Port Only	26 <sub>H</sub>	<b>119</b>
<b>Q3WBPVAO</b>	Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged	27 <sub>H</sub>	<b>119</b>
<b>IDTEP</b>	Input Double Tag Enable, and P0VID[11:4]	28 <sub>H</sub>	<b>120</b>
<b>ODTEP</b>	Output Double Tag Enable, and P1VID[11:4]	29 <sub>H</sub>	<b>120</b>
<b>OTBP</b>	Output Tag Bypass, and P2VID[11:4]	2A <sub>H</sub>	<b>121</b>
<b>P11_4</b>	P3VID[11:4], and P4VID[11:4]	2B <sub>H</sub>	<b>121</b>
<b>RACP</b>	Reserved Address Control, and P5VID[11:4]	2C <sub>H</sub>	<b>122</b>
<b>PHYC</b>	PHY Control Register	2D <sub>H</sub>	<b>122</b>
<b>ATET</b>	ADM TAG Ether Type	2E <sub>H</sub>	<b>123</b>
<b>PR</b>	PHY Restart Register	2F <sub>H</sub>	<b>124</b>
<b>MISC</b>	Miscellaneous Register	30 <sub>H</sub>	<b>124</b>
<b>BBC0</b>	Basic Bandwidth Control Register 0	31 <sub>H</sub>	<b>125</b>
<b>BBC1</b>	Basic Bandwidth Control Register 1	32 <sub>H</sub>	<b>126</b>
<b>BCE</b>	Bandwidth Control Enable Register	33 <sub>H</sub>	<b>127</b>
<b>EBC0</b>	Extended Bandwidth Control Register 0	34 <sub>H</sub>	<b>128</b>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<b>EBC1</b>	Extended Bandwidth Control Register 1	35 <sub>H</sub>	<b>129</b>
<b>EBC2</b>	Extended Bandwidth Control Register 2	36 <sub>H</sub>	<b>130</b>
<b>EBC3</b>	Extended Bandwidth Control Register 3	37 <sub>H</sub>	<b>131</b>
<b>EBC4</b>	Extended Bandwidth Control Register 4	38 <sub>H</sub>	<b>131</b>
<b>EBC5</b>	Extended Bandwidth Control Register 5	39 <sub>H</sub>	<b>132</b>
<b>DVMEBC6</b>	Default VLAN Member and Extended Bandwidth Control Register 6	3A <sub>H</sub>	<b>132</b>
<b>NS0</b>	New Storm Register 0	3B <sub>H</sub>	<b>133</b>
<b>NS1</b>	New Storm Register 1	3C <sub>H</sub>	<b>135</b>
<b>NRAC0</b>	New Reserve Address Control Register 0	3D <sub>H</sub>	<b>135</b>
<b>NRAC1</b>	New Reserve Address Control Register 1	3E <sub>H</sub>	<b>137</b>
<b>HIC</b>	Hardware IGMP Control Register	3F <sub>H</sub>	<b>138</b>
<b>VF0L</b>	VLAN Filter 0 Low	40 <sub>H</sub>	<b>139</b>
<b>VF0H</b>	VLAN Filter 0 High	41 <sub>H</sub>	<b>140</b>
<b>VF1L</b>	VLAN Filter 1 Low	42 <sub>H</sub>	<b>140</b>
<b>VF1H</b>	VLAN Filter 1 High	43 <sub>H</sub>	<b>141</b>
<b>VF2L</b>	VLAN Filter 2 Low	44 <sub>H</sub>	<b>140</b>
<b>VF2H</b>	VLAN Filter 2 High	45 <sub>H</sub>	<b>141</b>
<b>VF3L</b>	VLAN Filter 3 Low	46 <sub>H</sub>	<b>140</b>
<b>VF3H</b>	VLAN Filter 3 High	47 <sub>H</sub>	<b>141</b>
<b>VF4L</b>	VLAN Filter 4 Low	48 <sub>H</sub>	<b>140</b>
<b>VF4H</b>	VLAN Filter 4 High	49 <sub>H</sub>	<b>141</b>
<b>VF5L</b>	VLAN Filter 5 Low	4A <sub>H</sub>	<b>140</b>
<b>VF5H</b>	VLAN Filter 5 High	4B <sub>H</sub>	<b>141</b>
<b>VF6L</b>	VLAN Filter 6 Low	4C <sub>H</sub>	<b>140</b>
<b>VF6H</b>	VLAN Filter 6 High	4D <sub>H</sub>	<b>141</b>
<b>VF7L</b>	VLAN Filter 7 Low	4E <sub>H</sub>	<b>140</b>
<b>VF7H</b>	VLAN Filter 7 High	4F <sub>H</sub>	<b>141</b>
<b>VF8L</b>	VLAN Filter 8 Low	50 <sub>H</sub>	<b>140</b>
<b>VF8H</b>	VLAN Filter 8 High	51 <sub>H</sub>	<b>141</b>
<b>VF9L</b>	VLAN Filter 9 Low	52 <sub>H</sub>	<b>140</b>
<b>VF9H</b>	VLAN Filter 9 High	53 <sub>H</sub>	<b>141</b>
<b>VF10L</b>	VLAN Filter 10 Low	54 <sub>H</sub>	<b>140</b>
<b>VF10H</b>	VLAN Filter 10 High	55 <sub>H</sub>	<b>141</b>
<b>VF11L</b>	VLAN Filter 11 Low	56 <sub>H</sub>	<b>140</b>
<b>VF11H</b>	VLAN Filter 11 High	57 <sub>H</sub>	<b>141</b>
<b>VF12L</b>	VLAN Filter 12 Low	58 <sub>H</sub>	<b>140</b>
<b>VF12H</b>	VLAN Filter 12 High	59 <sub>H</sub>	<b>141</b>
<b>VF13L</b>	VLAN Filter 13 Low	5A <sub>H</sub>	<b>140</b>
<b>VF13H</b>	VLAN Filter 13 High	5B <sub>H</sub>	<b>141</b>
<b>VF14L</b>	VLAN Filter 14 Low	5C <sub>H</sub>	<b>140</b>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">VF14H</a>	VLAN Filter 14 High	5D <sub>H</sub>	<a href="#">141</a>
<a href="#">VF15L</a>	VLAN Filter 15 Low	5E <sub>H</sub>	<a href="#">140</a>
<a href="#">VF15H</a>	VLAN Filter 15 High	5F <sub>H</sub>	<a href="#">141</a>
<a href="#">TF0</a>	Type Filter 0	60 <sub>H</sub>	<a href="#">141</a>
<a href="#">TF1</a>	Type Filter 1	61 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF2</a>	Type Filter 2	62 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF3</a>	Type Filter 3	63 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF4</a>	Type Filter 4	64 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF5</a>	Type Filter 5	65 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF6</a>	Type Filter 6	66 <sub>H</sub>	<a href="#">142</a>
<a href="#">TF7</a>	Type Filter 7	67 <sub>H</sub>	<a href="#">142</a>
<a href="#">PF_1_0</a>	Protocol Filter 1 and 0	68 <sub>H</sub>	<a href="#">143</a>
<a href="#">PF_3_2</a>	Protocol Filter 3 and 2	68 <sub>H</sub>	<a href="#">143</a>
<a href="#">PF_5_4</a>	Protocol Filter 5 and 4	69 <sub>H</sub>	<a href="#">143</a>
<a href="#">PF_7_6</a>	Protocol Filter 7 and 6	6A <sub>H</sub>	<a href="#">143</a>
<a href="#">SPM0</a>	Service Priority Mapping 0	6C <sub>H</sub>	<a href="#">143</a>
<a href="#">SPM1</a>	Service Priority Mapping 1	6D <sub>H</sub>	<a href="#">144</a>
<a href="#">SPM2</a>	Service Priority Mapping 2	6E <sub>H</sub>	<a href="#">145</a>
<a href="#">SPM3</a>	Service Priority Mapping 3	6F <sub>H</sub>	<a href="#">146</a>
<a href="#">SPM4</a>	Service Priority Mapping 4	70 <sub>H</sub>	<a href="#">147</a>
<a href="#">SPM5</a>	Service Priority Mapping 5	71 <sub>H</sub>	<a href="#">148</a>
<a href="#">SPM6</a>	Service Priority Mapping 6	72 <sub>H</sub>	<a href="#">148</a>
<a href="#">SPM7</a>	Service Priority Mapping 7	73 <sub>H</sub>	<a href="#">149</a>
<a href="#">RA_01_00</a>	Reserve Action for 0180C2000001~0180C2000000	74 <sub>H</sub>	<a href="#">150</a>
<a href="#">RA_03_02</a>	Reserve Action for 0180C2000003~0180C2000002	75 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_05_04</a>	Reserve Action for 0180C2000005~0180C2000004	76 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_07_06</a>	Reserve Action for 0180C2000007~0180C2000006	77 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_09_08</a>	Reserve Action for 0180C2000009~0180C2000008	78 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_0B_0A</a>	Reserve Action for 0180C200000B~0180C200000A	79 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_0D_0C</a>	Reserve Action for 0180C200000D~0180C200000C	7A <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_0F_0E</a>	Reserve Action for 0180C200000F~0180C200000E	7B <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_11_10</a>	Reserve Action for 0180C2000011~0180C2000010	7C <sub>H</sub>	<a href="#">152</a>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">RA_13_12</a>	Reserve Action for 0180C2000013~0180C2000012	7D <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_15_14</a>	Reserve Action for 0180C2000015~0180C2000014	7E <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_17_16</a>	Reserve Action for 0180C2000017~0180C2000016	7F <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_19_18</a>	Reserve Action for 0180C2000019~0180C2000018	80 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_1B_1A</a>	Reserve Action for 0180C200001B~0180C200001A	81 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_1D_1C</a>	Reserve Action for 0180C200001D~0180C200001C	82 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_1F_1E</a>	Reserve Action for 0180C200001F~0180C200001E	83 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_21_20</a>	Reserve Action for 0180C2000021~0180C2000020	84 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_23_22</a>	Reserve Action for 0180C2000023~0180C2000022	85 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_25_24</a>	Reserve Action for 0180C2000025~0180C2000024	86 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_27_26</a>	Reserve Action for 0180C2000027~0180C2000026	87 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_29_28</a>	Reserve Action for 0180C2000029~0180C2000028	88 <sub>H</sub>	<a href="#">152</a>
<a href="#">RA_2B_2A</a>	Reserve Action for 0180C200002B~0180C200002A	89 <sub>H</sub>	<a href="#">153</a>
<a href="#">RA_2D_2C</a>	Reserve Action for 0180C200002D~0180C200002C	8A <sub>H</sub>	<a href="#">153</a>
<a href="#">RA_2F_2E</a>	Reserve Action for 0180C200002F~0180C200002E	8B <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF0</a>	TCP/UDP Filter 0	8C <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF1</a>	TCP/UDP Filter 1	8D <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF2</a>	TCP/UDP Filter 2	8E <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF3</a>	TCP/UDP Filter 3	8F <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF4</a>	TCP/UDP Filter 4	90 <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF5</a>	TCP/UDP Filter 5	91 <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF6</a>	TCP/UDP Filter 6	92 <sub>H</sub>	<a href="#">153</a>
<a href="#">TUF7</a>	TCP/UDP Filter 7	93 <sub>H</sub>	<a href="#">153</a>
<a href="#">TFA</a>	Type Filter Action	94 <sub>H</sub>	<a href="#">153</a>
<a href="#">PFA</a>	Protocol Filter Action	95 <sub>H</sub>	<a href="#">154</a>
<a href="#">TUA0</a>	TCP/UDP Action 0	96 <sub>H</sub>	<a href="#">155</a>
<a href="#">TUA1</a>	TCP/UDP Action 1	97 <sub>H</sub>	<a href="#">156</a>
<a href="#">TUA2</a>	TCP/UDP Action 2	98 <sub>H</sub>	<a href="#">157</a>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<b>EICSTIC</b>	Extended IGMP Control/Special Tag Insert Control	99 <sub>H</sub>	<b>158</b>
<b>IE</b>	Interrupt Enable Register	9A <sub>H</sub>	<b>159</b>
<b>IS</b>	Interrupt Status Register	9B <sub>H</sub>	<b>160</b>
<b>SC</b>	Security Control Register	9C <sub>H</sub>	<b>160</b>
<b>CI0</b>	Chip Identifier 0	A0 <sub>H</sub>	<b>161</b>
<b>CI1</b>	Chip Identifier 1	A1 <sub>H</sub>	<b>161</b>
<b>PS0</b>	Port Status 0	A2 <sub>H</sub>	<b>161</b>
<b>PS1</b>	Port Status 1	A3 <sub>H</sub>	<b>162</b>
<b>PS2</b>	Port Status 2	A4 <sub>H</sub>	<b>163</b>
<b>PS3</b>	Port Status 3	A5 <sub>H</sub>	<b>164</b>
<b>CB0</b>	Cable Broken 0	A6 <sub>H</sub>	<b>164</b>
<b>CB1</b>	Cable Broken 1	A7 <sub>H</sub>	<b>165</b>
<b>CL0</b>	Port 0 Receive Packet Counter Low	A8 <sub>H</sub>	<b>165</b>
<b>CH0</b>	Port 0 Receive Packet Counter High	A9 <sub>H</sub>	<b>166</b>
<b>CL1</b>	Port 1 Receive Packet Counter Low	AC <sub>H</sub>	<b>166</b>
<b>CH1</b>	Port 1 Receive Packet Counter High	AD <sub>H</sub>	<b>167</b>
<b>CL2</b>	Port 2 Receive Packet Counter Low	B0 <sub>H</sub>	<b>166</b>
<b>CH2</b>	Port 2 Receive Packet Counter High	B1 <sub>H</sub>	<b>167</b>
<b>CL3</b>	Port 3 Receive Packet Counter Low	B4 <sub>H</sub>	<b>166</b>
<b>CH3</b>	Port 3 Receive Packet Counter High	B5 <sub>H</sub>	<b>167</b>
<b>CL4</b>	Port 4 Receive Packet Counter Low	B6 <sub>H</sub>	<b>166</b>
<b>CH4</b>	Port 4 Receive Packet Counter High	B7 <sub>H</sub>	<b>167</b>
<b>CL5</b>	Port 5 Receive Packet Counter Low	B8 <sub>H</sub>	<b>166</b>
<b>CH5</b>	Port 5 Receive Packet Counter High	B9 <sub>H</sub>	<b>167</b>
<b>CL6</b>	Port 0 Receive Packet Byte Count Low	BA <sub>H</sub>	<b>166</b>
<b>CH6</b>	Port 0 Receive Packet Byte Count High	BB <sub>H</sub>	<b>167</b>
<b>CL7</b>	Port 1 Receive Packet Byte Count Low	BE <sub>H</sub>	<b>166</b>
<b>CH7</b>	Port 1 Receive Packet Byte Count High	BF <sub>H</sub>	<b>167</b>
<b>CL8</b>	Port 2 Receive Packet Byte Count Low	C2 <sub>H</sub>	<b>166</b>
<b>CH8</b>	Port 2 Receive Packet Byte Count High	C3 <sub>H</sub>	<b>167</b>
<b>CL9</b>	Port 3 Receive Packet Byte Count Low	C6 <sub>H</sub>	<b>166</b>
<b>CH9</b>	Port 3 Receive Packet Byte Count High	C7 <sub>H</sub>	<b>167</b>
<b>CL10</b>	Port 4 Receive Packet Byte Count Low	C8 <sub>H</sub>	<b>166</b>
<b>CH10</b>	Port 4 Receive Packet Byte Count High	C9 <sub>H</sub>	<b>167</b>
<b>CL11</b>	Port 5 Receive Packet Byte Count Low	CA <sub>H</sub>	<b>166</b>
<b>CH11</b>	Port 5 Receive Packet Byte Count High	CB <sub>H</sub>	<b>167</b>
<b>CL12</b>	Port 0 Transmit Packet Count Low	CC <sub>H</sub>	<b>166</b>
<b>CH12</b>	Port 0 Transmit Packet Count High	CD <sub>H</sub>	<b>167</b>
<b>CL13</b>	Port 1 Transmit Packet Count Low	D0 <sub>H</sub>	<b>166</b>
<b>CH13</b>	Port 1 Transmit Packet Count High	D1 <sub>H</sub>	<b>167</b>
<b>CL14</b>	Port 2 Transmit Packet Count Low	D4 <sub>H</sub>	<b>166</b>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">CH14</a>	Port 2 Transmit Packet Count High	D5 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL15</a>	Port 3 Transmit Packet Count Low	D8 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH15</a>	Port 3 Transmit Packet Count High	D9 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL16</a>	Port 4 Transmit Packet Count Low	DA <sub>H</sub>	<a href="#">166</a>
<a href="#">CH16</a>	Port 4 Transmit Packet Count High	DB <sub>H</sub>	<a href="#">167</a>
<a href="#">CL17</a>	Port 5 Transmit Packet Count Low	DC <sub>H</sub>	<a href="#">166</a>
<a href="#">CH17</a>	Port 5 Transmit Packet Count High	DD <sub>H</sub>	<a href="#">167</a>
<a href="#">CL18</a>	Port 0 Transmit Packet Byte Count Low	DE <sub>H</sub>	<a href="#">166</a>
<a href="#">CH18</a>	Port 0 Transmit Packet Byte Count High	DF <sub>H</sub>	<a href="#">167</a>
<a href="#">CL19</a>	Port 1 Transmit Packet Byte Count Low	E2 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH19</a>	Port 1 Transmit Packet Byte Count High	E3 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL20</a>	Port 2 Transmit Packet Byte Count Low	E6 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH20</a>	Port 2 Transmit Packet Byte Count High	E7 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL21</a>	Port 3 Transmit Packet Byte Count Low	EA <sub>H</sub>	<a href="#">166</a>
<a href="#">CH21</a>	Port 3 Transmit Packet Byte Count High	EB <sub>H</sub>	<a href="#">167</a>
<a href="#">CL22</a>	Port 4 Transmit Packet Byte Count Low	EC <sub>H</sub>	<a href="#">166</a>
<a href="#">CH22</a>	Port 4 Transmit Packet Byte Count High	ED <sub>H</sub>	<a href="#">167</a>
<a href="#">CL23</a>	Port 5 Transmit Packet Byte Count Low	EE <sub>H</sub>	<a href="#">166</a>
<a href="#">CH23</a>	Port 5 Transmit Packet Byte Count High	EF <sub>H</sub>	<a href="#">167</a>
<a href="#">CL24</a>	Port 0 Collision Count Low	F0 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH24</a>	Port 0 Collision Count High	F1 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL25</a>	Port 1 Collision Count Low	F4 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH25</a>	Port 1 Collision Count High	F5 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL26</a>	Port 2 Collision Count Low	F8 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH26</a>	Port 2 Collision Count High	F9 <sub>H</sub>	<a href="#">167</a>
<a href="#">CL27</a>	Port 3 Collision Count Low	FC <sub>H</sub>	<a href="#">166</a>
<a href="#">CH27</a>	Port 3 Collision Count High	FD <sub>H</sub>	<a href="#">167</a>
<a href="#">CL28</a>	Port 4 Collision Count Low	FE <sub>H</sub>	<a href="#">166</a>
<a href="#">CH28</a>	Port 4 Collision Count High	FF <sub>H</sub>	<a href="#">167</a>
<a href="#">CL29</a>	Port 5 Collision Count Low	100 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH29</a>	Port 5 Collision Count High	101 <sub>H</sub>	<a href="#">168</a>
<a href="#">CL30</a>	Port 0 Error Count Low	102 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH30</a>	Port 0 Error Count High	103 <sub>H</sub>	<a href="#">168</a>
<a href="#">CL31</a>	Port 1 Error Count Low	106 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH31</a>	Port 1 Error Count High	107 <sub>H</sub>	<a href="#">168</a>
<a href="#">CL32</a>	Port 2 Error Count Low	10A <sub>H</sub>	<a href="#">166</a>
<a href="#">CH32</a>	Port 2 Error Count High	10B <sub>H</sub>	<a href="#">168</a>
<a href="#">CL33</a>	Port 3 Error Count Low	10E <sub>H</sub>	<a href="#">166</a>
<a href="#">CH33</a>	Port 3 Error Count High	10F <sub>H</sub>	<a href="#">168</a>
<a href="#">CL34</a>	Port 4 Error Count Low	110 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH34</a>	Port 4 Error Count High	111 <sub>H</sub>	<a href="#">168</a>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">CL35</a>	Port 5 Error Count Low	112 <sub>H</sub>	<a href="#">166</a>
<a href="#">CH35</a>	Port 5 Error Count High	113 <sub>H</sub>	<a href="#">168</a>
<a href="#">OFF0</a>	Over-Flow Flag 0	114 <sub>H</sub>	<a href="#">168</a>
<a href="#">OFF1</a>	Over-Flow Flag 1	115 <sub>H</sub>	<a href="#">169</a>
<a href="#">OFF2</a>	Over-Flow Flag 2	116 <sub>H</sub>	<a href="#">169</a>
<a href="#">OFF3</a>	Over-Flow Flag 3	117 <sub>H</sub>	<a href="#">170</a>
<a href="#">OFF4</a>	Over-Flow Flag 4	118 <sub>H</sub>	<a href="#">171</a>
<a href="#">OFF5</a>	Over-Flow Flag 5	119 <sub>H</sub>	<a href="#">172</a>
<a href="#">HSL</a>	Hardware Setting Low Register	130 <sub>H</sub>	<a href="#">173</a>
<a href="#">HSH</a>	Hardware Setting High Register	131 <sub>H</sub>	<a href="#">173</a>
<a href="#">AA1</a>	Assign Address [15:0] Register	132 <sub>H</sub>	<a href="#">174</a>
<a href="#">AA2</a>	Assign Address [31:16] Register	133 <sub>H</sub>	<a href="#">174</a>
<a href="#">AA3</a>	Assign Address [47:32] Register	134 <sub>H</sub>	<a href="#">176</a>
<a href="#">AO</a>	Assign Option Register	135 <sub>H</sub>	<a href="#">176</a>
<a href="#">MIRR0</a>	Mirror Register 0	136 <sub>H</sub>	<a href="#">177</a>
<a href="#">MIRR1</a>	Mirror Register 1	137 <sub>H</sub>	<a href="#">178</a>
<a href="#">SVP</a>	Security Violation Port	138 <sub>H</sub>	<a href="#">179</a>
<a href="#">SS0</a>	Security Status 0	139 <sub>H</sub>	<a href="#">179</a>
<a href="#">SS1</a>	Security Status 1	13A <sub>H</sub>	<a href="#">180</a>
<a href="#">FLAS</a>	First Lock Address Search	13B <sub>H</sub>	<a href="#">180</a>
<a href="#">FLA1</a>	First Lock Address [15:0]	13C <sub>H</sub>	<a href="#">182</a>
<a href="#">FLA2</a>	First Lock Address [31:16]	13D <sub>H</sub>	<a href="#">182</a>
<a href="#">FLA3</a>	First Lock Address [47:32]	13E <sub>H</sub>	<a href="#">182</a>
<a href="#">FLF</a>	First Lock FID	13F <sub>H</sub>	<a href="#">183</a>
<a href="#">CCL</a>	Counter Control Low Register	140 <sub>H</sub>	<a href="#">183</a>
<a href="#">CCH</a>	Counter Control High Register	141 <sub>H</sub>	<a href="#">185</a>
<a href="#">CSL</a>	Counter Status Low Register	142 <sub>H</sub>	<a href="#">185</a>
<a href="#">CSH</a>	Counter Status High Register	143 <sub>H</sub>	<a href="#">185</a>
<a href="#">PHY_C0</a>	PHY Control Register of Port 0	200 <sub>H</sub>	<a href="#">186</a>
<a href="#">PHY_S0</a>	PHY Status Register of Port 0	201 <sub>H</sub>	<a href="#">189</a>
<a href="#">PHY_I0_A</a>	PHY Identifier Register of Port 0 (A)	202 <sub>H</sub>	<a href="#">190</a>
<a href="#">PHY_I0_B</a>	PHY Identifier Register of Port 0 (B)	203 <sub>H</sub>	<a href="#">191</a>
<a href="#">ANAP0</a>	Auto Negotiation Advertisement Register of Port 0	204 <sub>H</sub>	<a href="#">192</a>
<a href="#">ANLPA0</a>	Auto Negotiation Link Partner Ability Register of Port 0	205 <sub>H</sub>	<a href="#">193</a>
<a href="#">ANE0</a>	Auto Negotiation Expansion Register of Port 0	206 <sub>H</sub>	<a href="#">194</a>
<a href="#">NPT0</a>	Next Page Transmit Register of Port 0	207 <sub>H</sub>	<a href="#">195</a>
<a href="#">LPNP0</a>	Link Partner Next Page Register of Port 0	208 <sub>H</sub>	<a href="#">196</a>
<a href="#">PHY_C1</a>	PHY Control Register of Port 1	220 <sub>H</sub>	<a href="#">188</a>
<a href="#">PHY_S1</a>	PHY Status Register of Port 1	221 <sub>H</sub>	<a href="#">190</a>
<a href="#">PHY_I1_A</a>	PHY Identifier Register of Port 1 (A)	222 <sub>H</sub>	<a href="#">191</a>

**Table 52 Registers Overview (cont'd)**

<b>Register Short Name</b>	<b>Register Long Name</b>	<b>Offset Address</b>	<b>Page Number</b>
<a href="#">PHY_I1_B</a>	PHY Identifier Register of Port 1 (B)	223 <sub>H</sub>	<a href="#">192</a>
<a href="#">ANAP1</a>	Auto Negotiation Advertisement Register of Port 1	224 <sub>H</sub>	<a href="#">193</a>
<a href="#">ANLPA1</a>	Auto Negotiation Link Partner Ability Register of Port 1	225 <sub>H</sub>	<a href="#">194</a>
<a href="#">ANE1</a>	Auto Negotiation Expansion Register of Port 1	226 <sub>H</sub>	<a href="#">195</a>
<a href="#">NPT1</a>	Next Page Transmit Register of Port 1	227 <sub>H</sub>	<a href="#">196</a>
<a href="#">LPNP1</a>	Link Partner Next Page Register of Port 1	228 <sub>H</sub>	<a href="#">197</a>
<a href="#">PHY_C2</a>	PHY Control Register of Port 2	240 <sub>H</sub>	<a href="#">188</a>
<a href="#">PHY_S2</a>	PHY Status Register of Port 2	241 <sub>H</sub>	<a href="#">190</a>
<a href="#">PHY_I2_A</a>	PHY Identifier Register of Port 2 (A)	242 <sub>H</sub>	<a href="#">191</a>
<a href="#">PHY_I2_B</a>	PHY Identifier Register of Port 2 (B)	243 <sub>H</sub>	<a href="#">192</a>
<a href="#">ANAP2</a>	Auto Negotiation Advertisement Register of Port 2	244 <sub>H</sub>	<a href="#">193</a>
<a href="#">ANLPA2</a>	Auto Negotiation Link Partner Ability Register of Port 2	245 <sub>H</sub>	<a href="#">194</a>
<a href="#">ANE2</a>	Auto Negotiation Expansion Register of Port 2	246 <sub>H</sub>	<a href="#">195</a>
<a href="#">NPT2</a>	Next Page Transmit Register of Port 2	247 <sub>H</sub>	<a href="#">196</a>
<a href="#">LPNP2</a>	Link Partner Next Page Register of Port 2	248 <sub>H</sub>	<a href="#">197</a>
<a href="#">PHY_C3</a>	PHY Control Register of Port 3	260 <sub>H</sub>	<a href="#">188</a>
<a href="#">PHY_S3</a>	PHY Status Register of Port 3	261 <sub>H</sub>	<a href="#">190</a>
<a href="#">PHY_I3_A</a>	PHY Identifier Register of Port 3 (A)	262 <sub>H</sub>	<a href="#">191</a>
<a href="#">PHY_I3_B</a>	PHY Identifier Register of Port 3 (B)	263 <sub>H</sub>	<a href="#">192</a>
<a href="#">ANAP3</a>	Auto Negotiation Advertisement Register of Port 3	264 <sub>H</sub>	<a href="#">193</a>
<a href="#">ANLPA3</a>	Auto Negotiation Link Partner Ability Register of Port 3	265 <sub>H</sub>	<a href="#">194</a>
<a href="#">ANE3</a>	Auto Negotiation Expansion Register of Port 3	266 <sub>H</sub>	<a href="#">195</a>
<a href="#">NPT3</a>	Next Page Transmit Register of Port 3	267 <sub>H</sub>	<a href="#">196</a>
<a href="#">LPNP3</a>	Link Partner Next Page Register of Port 3	268 <sub>H</sub>	<a href="#">197</a>
<a href="#">PHY_C4</a>	PHY Control Register of Port 4	280 <sub>H</sub>	<a href="#">188</a>
<a href="#">PHY_S4</a>	PHY Status Register of Port 4	281 <sub>H</sub>	<a href="#">190</a>
<a href="#">PHY_I4_A</a>	PHY Identifier Register of Port 4 (A)	282 <sub>H</sub>	<a href="#">191</a>
<a href="#">PHY_I4_B</a>	PHY Identifier Register of Port 4 (B)	283 <sub>H</sub>	<a href="#">192</a>
<a href="#">ANAP4</a>	Auto Negotiation Advertisement Register of Port 4	284 <sub>H</sub>	<a href="#">193</a>
<a href="#">ANLPA4</a>	Auto Negotiation Link Partner Ability Register of Port 4	285 <sub>H</sub>	<a href="#">194</a>
<a href="#">ANE4</a>	Auto Negotiation Expansion Register of Port 4	286 <sub>H</sub>	<a href="#">195</a>
<a href="#">NPT4</a>	Next Page Transmit Register of Port 4	287 <sub>H</sub>	<a href="#">196</a>
<a href="#">LPNP4</a>	Link Partner Next Page Register of Port 4	288 <sub>H</sub>	<a href="#">197</a>

The register is addressed wordwise.



**Table 53 Register Access Types**

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latches high signal at high level, cleared on read	SW can read the register
Latch low, self clearing	llsc	Latches high signal at low-level, cleared on read	SW can read the register
Latch high, mask clearing	lhmk	Latches high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latches high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

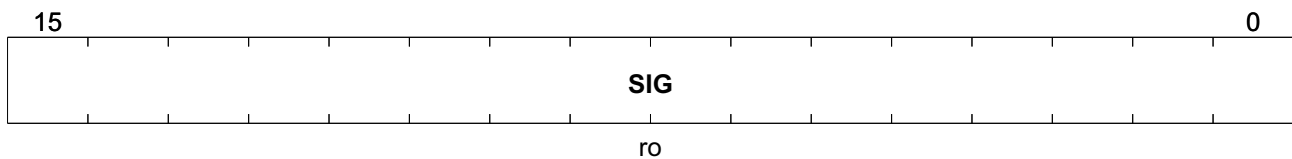
**Table 54 Registers Clock Domains**

Clock Short Name	Description
-	-

## 4.1 EEPROM Basic Registers

### Signature Register

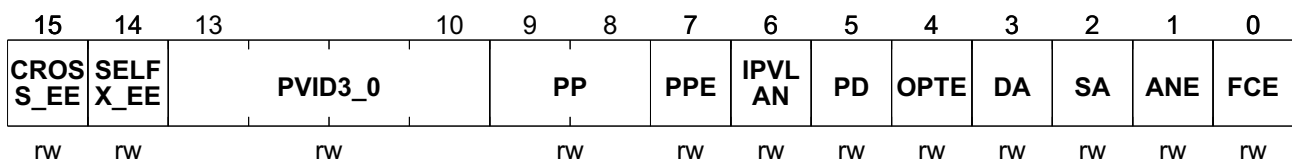
<b>SIG</b>	<b>Offset</b>	<b>Reset Value</b>
Signature Register	00 <sub>H</sub>	4154 <sub>H</sub>



Field	Bits	Type	Description
SIG	15:0	ro	<b>Signature</b> The value must be 4154 <sub>H</sub> . Samurai-6M/6MX (ADM6996M/MX) uses this value to check if EEPROM is attached. If the value in the EEPROM is not equal to 4154 <sub>H</sub> , Samurai-6M/6MX (ADM6996M/MX) will stop loading the EEPROM even if EEPROM is attached and Samurai-6M/6MX (ADM6996M/MX) will use the default value inside the chip to initialize.

### P0 Basic Control Register

<b>P0BC</b>	<b>Offset</b>	<b>Reset Value</b>
P0 Basic Control Register	01 <sub>H</sub>	040F <sub>H</sub>



Field	Bits	Type	Description
CROSS_EE	15	rw	<p><b>Crossover Auto Detect Enable</b></p> <p>This bit is used together with the value (cross_hw) on the pin <b>EESK/SDC</b> during the power on reset and the value (wait_init) on the pin <b>WAIT_INIT</b> during the normal mode to decide if PHY enables this function. This bit is useless in Port 5.</p> <p>Combine with wait_init and cross_hw, the crossover auto detect capability is summarized as below :</p> <p>{wait_init, cross_hw, cross_ee} Description</p> <p>1x1<sub>B</sub> This port will enable Crossover Auto Detect Enable function</p> <p>1x0<sub>B</sub> This port will disable Crossover Auto Detect Enable function</p> <p>01x<sub>B</sub> This port will enable Crossover Auto Detect Enable function</p> <p>000<sub>B</sub> This port will disable Crossover Auto Detect Enable function</p> <p>001<sub>B</sub> This port will enable Crossover Auto Detect Enable function</p>
SELFX_EE	14	rw	<p><b>Select FX</b></p> <p>This bit is used together with the value (p4fx_hw) on the pin <b>P4FX</b> during the power on reset to decide if the PHY operates on the fiber mode. This bit is useless in Port 5. Port 0, 1, 2, 3: follow selfx_ee Description and Port 4: follow {p4fx_hw, selfx_ee} Description</p> <p>1x<sub>B</sub> Port 4: Port 4 will operate in the fiber mode</p> <p>00<sub>B</sub> Port 4: Port 4 will operate in the twisted mode</p> <p>01<sub>B</sub> Port 4: Port 4 will operate in the fiber mode</p>
PVID3_0	13:10	rw	<p><b>Private VID</b></p> <p>See 0028<sub>H</sub> ~ 002C<sub>H</sub> to find the other PVID [11:4]</p>
PP	9:8	rw	<p><b>Port Priority</b></p> <p>00<sub>B</sub> Assign packets to Queue 0</p> <p>01<sub>B</sub> Assign packets to Queue 1</p> <p>10<sub>B</sub> Assign packets to Queue 2</p> <p>11<sub>B</sub> Assign packets to Queue 3</p>
PPE	7	rw	<p><b>Port Priority Enable</b></p> <p>0<sub>B</sub> The port priority is disabled</p> <p>1<sub>B</sub> The port priority is enabled</p>
IPVLAN	6	rw	<p><b>IP over VLAN PRI</b></p> <p>0<sub>B</sub> Use the priority bits in the tag header to assign the priority queue</p> <p>1<sub>B</sub> Use the IP PRI to assign the priority queue</p>
PD	5	rw	<p><b>Port Disable</b></p> <p>0<sub>B</sub> Port 0, 1, 2, 3, 4: PHY works normally. Port 5: Port 5 works normally</p> <p>1<sub>B</sub> Port 0, 1, 2, 3, 4. PHY is disabled. Port 5: Port 5 is forced to link down</p>
OPTE	4	rw	<p><b>Output Packet Tagging Enable</b></p> <p>0<sub>B</sub> Untagged packets are transmitted</p> <p>1<sub>B</sub> Tagged packets are transmitted</p>
DA	3	rw	<p><b>Duplex Ability</b></p> <p>It is useless in Port 5.</p> <p>0<sub>B</sub> Recommend PHY to work in the half duplex mode</p> <p>1<sub>B</sub> Recommend PHY to work in the full duplex mode</p>

Registers Description

Field	Bits	Type	Description
SA	2	rw	<b>Speed Ability</b> It is useless in Port 5. 0 <sub>B</sub> Recommend PHY to work in the 10M mode 1 <sub>B</sub> Recommend PHY to work in the 100M mode
ANE	1	rw	<b>Auto Negotiation Enable</b> It is useless in Port 5. 0 <sub>B</sub> Recommend PHY to work without Auto Negotiation 1 <sub>B</sub> Recommend PHY to work with Auto Negotiation, when the value on the pin DUPCOL0 during the power on reset is 1
FCE	0	rw	<b>Flow Control Enable</b> 0 <sub>B</sub> Recommend MAC to work without Pause or Back Pressure 1 <sub>B</sub> In full duplex, recommend MAC to work with Pause when the value on the TXD0 during the power on reset is 1. In half duplex, recommend MAC to work with Back Pressure when the value on the DUPCOL2 during the power on reset is 1

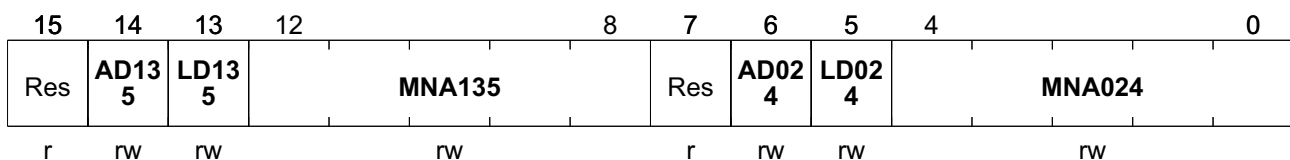
Similar Registers

Table 55 P1~P5 Basic Control Registers

Register Short Name	Register Long Name	Offset Address	Page Number
P1BC	P1 Basic Control Register	03 <sub>H</sub>	
P2BC	P2 Basic Control Register	05 <sub>H</sub>	
P3BC	P3 Basic Control Register	07 <sub>H</sub>	
P4BC	P4 Basic Control Register	08 <sub>H</sub>	
P5BC	P5 Basic Control Register	09 <sub>H</sub>	

P0 Extended Control Register

<b>P0EC</b>	<b>Offset</b>	<b>Reset Value</b>
<b>P0 Extended Control Register</b>	<b>02<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
AD135	14	rw	<b>Aging Disable</b> P1, P3, and P5. 0 <sub>B</sub> Aging function is enabled 1 <sub>B</sub> Aging function is disabled



Field	Bits	Type	Description
ERCMPH	15:12	rw	<b>Earlier Cycles for Transmission</b> It means the earlier cycles for transmission used in Samurai-6M/6MX (ADM6996M/MX). It is for the engineer debug purpose.
PCR	11	rw	<b>Priority Change Rule</b> 0 <sub>B</sub> Use VLAN_PRI field in the matched VLAN filter 1 <sub>B</sub> Reverse PRI in the same way as untagged packet
PCE	10	rw	<b>Priority Change Enable</b> 0 <sub>B</sub> Do not change the priority in the tag header 1 <sub>B</sub> Change the priority field in the tag header
RVID0	9	rw	<b>Replace VID0</b> 0 <sub>B</sub> Do not replace 1 <sub>B</sub> Replace
RVID1	8	rw	<b>Replace VID1</b> 0 <sub>B</sub> Do not replace 1 <sub>B</sub> Replace
RVIDFFF	7	rw	<b>Replace VIDFFF</b> 0 <sub>B</sub> Do not replace 1 <sub>B</sub> Replace
DFID	6:3	rw	<b>Default FID</b> See <a href="#">Chapter 3.1.14.7 FID and VLAN Boundary</a> for more detailed information.
NTTE	2	rw	<b>New Transmit Tag Enable</b> 0 <sub>B</sub> Use old 1 <sub>B</sub> Use new
TU	1	rw	<b>TOS Using</b> 0 <sub>B</sub> Use the most significant 6 bits of the TOS field in the IPV4 header to map the priority queue 1 <sub>B</sub> Use the most significant 3 bits of the TOS field in the IPV4 header to map the priority queue
PM	0	rw	<b>PPPOE Manage</b> When the port is configured as PPPOE Only, the port will only transmit the PPPOE packets. But when the packet is a management one, users could configure PPPOE Manage to 1 <sub>B</sub> to transmit this packet on the PPPOE Only port even if it is not a PPPOE packet. Samurai-6M/6MX (ADM6996M/MX) identifies packets with Ether-Type = 8863 <sub>H</sub> or 8864 <sub>H</sub> as the PPPOE packet.

### System Control Register 1

SC1	Offset	Reset Value
System Control Register 1	0B <sub>H</sub>	8001 <sub>H</sub>

Registers Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFEFD	IF	ASC	SIC	SIM	SIA	CMS	TE	TSIE	CPDC	SVOR	SVOA	SVOS	SVOD	NE	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DFEFD	15	rw	<b>Disable Far-End-Fault Detection</b> 0 <sub>B</sub> Far-End-Fault detection is enabled 1 <sub>B</sub> Far-End-Fault detection is disabled
IF	14	rw	<b>Input Filter</b> 0 <sub>B</sub> Discards packets directly when storming or the lack of input buffers 1 <sub>B</sub> Forwards packets to the un-congested port when storming or the lack of input buffers
ASC	13:12	rw	<b>Additional Snooping Control</b> These bits are used when the packets on the incoming port with the Ethernet destination address = 01005Exxxxxx <sub>H</sub> /3333xxxxx <sub>H</sub> are not IGMP_IP/MLD_IPV/MLD_IPV6 packets and not found in the learning table or the hardware IGMP table. 00 <sub>B</sub> As normal multicast packets 01 <sub>B</sub> Dropped 10 <sub>B</sub> Send to CPU if the receiving port is non-CPU port or send to Multicast Portmap if the receiving is the CPU port 11 <sub>B</sub> Reserved
SIC	11	rw	<b>Source Intrusion Condition</b> 0 <sub>B</sub> Learning table source violation does not consider the port match 1 <sub>B</sub> Learning table source violation takes the port match into consideration
SIM	10	rw	<b>Source Intrusion Must</b> 0 <sub>B</sub> Learning table source violation will be effective in the following conditions. (1) The packets are not the management packets. (2) The packets are the management packets but Source Violation Over Reserve ( <b>SVOR</b> ) is 1 <sub>B</sub> 1 <sub>B</sub> Must follow the learning table source violation rules
SIA	9	rw	<b>Source Intrusion Action</b> 0 <sub>B</sub> Discarded 1 <sub>B</sub> Send to the CPU port
CMS	8	rw	<b>Carrier Mask Select (Reserved for test)</b> 0 <sub>B</sub> Mask CRS of 4 Cycles 1 <sub>B</sub> Mask CRS of 5 Cycles
TE	7	rw	<b>Port 3 and Port 4 Trunk Enable</b> 0 <sub>B</sub> No trunk is enabled 1 <sub>B</sub> Port 3 and Port 4 are trunked
TSIE	6	rw	<b>Transmit Short IPG Enable</b> 0 <sub>B</sub> 96 bits time of IPG is used 1 <sub>B</sub> 88/96 bits time of IPG is used

Registers Description

Field	Bits	Type	Description
CPDC	5	rw	<b>CPU Port Doesn't Check</b> CPU Port doesn't check CRC, for packets with Special Tag. 0 <sub>B</sub> Checks 1 <sub>B</sub> Doesn't Check
SVOR	4	rw	<b>Source Violation Over Reserve</b> This bit is used when the management packet with DA = 0180C20000xx <sub>H</sub> violates the source rule. 0 <sub>B</sub> Source violation doesn't change the forwarding algorithm 1 <sub>B</sub> Source violation will change the forwarding algorithm
SVOA	3	rw	<b>Source Violation Over ARP/RARP</b> This bit is used when the ARP/RARP packet classified as management that violates the source rule. 0 <sub>B</sub> Source violation doesn't change the forwarding algorithm 1 <sub>B</sub> Source violation will change the forwarding algorithm
SVOS	2	rw	<b>Source Violation Over Snooping</b> This bit is used when the MLD_IPV6/MLD_IP/IGMP/IP packet classified as management that violates the source rule. 0 <sub>B</sub> Source violation doesn't change the forwarding algorithm 1 <sub>B</sub> Source violation will change the forwarding algorithm
SVOD	1	rw	<b>Source Violation Over Default</b> This bit is used when the packet that is not the same as the above and it is classified as management that violates the source rule. 0 <sub>B</sub> Source violation doesn't change the forwarding algorithm 1 <sub>B</sub> Source violation will change the forwarding algorithm
NE	0	rw	<b>New EEPROM</b> 0 <sub>B</sub> Use old EEPROM functions 1 <sub>B</sub> New EEPROM function is enabled

Multicast Snooping Register

MS Offset Reset Value  
 Multicast Snooping Register 0C<sub>H</sub> 0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCPA	SCPPE	SCPP	SCPTTH	SCPTC	SCPTM	SCPTS	TMI6P	TMIP	TIP	HIPI	HISE	HIDRE			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw



Field	Bits	Type	Description
SCPA	15:14	rw	<b>Snooping Control Packet Action</b> 00 <sub>B</sub> IGMP Portmap is 000000 <sub>B</sub> 01 <sub>B</sub> IGMP Portmap is the Multicast Portmap 10 <sub>B</sub> If the incoming port is not the CPU port, then the IGMP Portmap is the CPU port. If the incoming port is the CPU port, then the IGMP Portmap is the Multicast Portmap except the CPU port 11 <sub>B</sub> If the incoming port is not the CPU port, then the Multicast Portmap is the CPU port. If the incoming port is the CPU port, then the Multicast Portmap is the default output ports except the CPU port
SCPPE	13	rw	<b>Snooping Control Packet Priority Enable</b> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
SCPP	12:11	rw	<b>Snooping Control Packet Priority</b> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
SCPTTH	10:9	rw	<b>Snooping Control Packet Transmission Tag Handle</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
SCPTC	8	rw	<b>Snooping Control Packet Treated as Cross_VLAN Packet</b> 0 <sub>B</sub> Doesn't identify 1 <sub>B</sub> Identifies as the cross_VLAN packet
SCPTM	7	rw	<b>Snooping Control Packet Treated as Management Packet</b> 0 <sub>B</sub> Doesn't identify 1 <sub>B</sub> Identifies as the management packet
SCPTS	6	rw	<b>Snooping Control Packet Treated as Span Packet</b> 0 <sub>B</sub> Doesn't identify 1 <sub>B</sub> Identifies as the span packet
TMI6P	5	rw	<b>Trap MLD_IPV6 Packet</b> 0 <sub>B</sub> Doesn't trap 1 <sub>B</sub> Traps
TMIP	4	rw	<b>Trap MLD_IP Packet</b> 0 <sub>B</sub> Doesn't trap 1 <sub>B</sub> Traps
TIP	3	rw	<b>Trap IGMP_IP Packet</b> 0 <sub>B</sub> Doesn't Trap 1 <sub>B</sub> Trasp
HIPI	2	rw	<b>Hardware IGMP Packet Ignore CPU Port</b> 0 <sub>B</sub> IGMP packet forwards to CPU also when Hardware IGMP Snooping is enabled 1 <sub>B</sub> IGMP packet doesn't forward to CPU when Hardware IGMP Snooping is enabled

Registers Description

Field	Bits	Type	Description
HISE	1	rw	<b>Hardware IGMP Snooping Enable</b> 0 <sub>B</sub> Disable Hardware IGMP Snooping 1 <sub>B</sub> Enable Hardware IGMP Snooping
HIDRE	0	rw	<b>Hardware IGMP Default Router Enable</b> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable



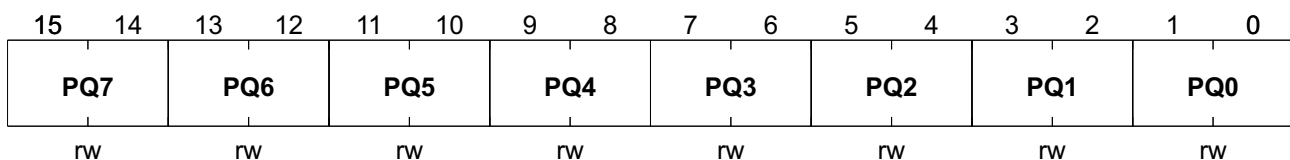


Registers Description

Field	Bits	Type	Description
PQ5	11:10	rw	<b>Priority Queue 5</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 101 <sub>B</sub> are received on the port.
PQ4	9:8	rw	<b>Priority Queue 4</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 100 <sub>B</sub> are received on the port.
PQ3	7:6	rw	<b>Priority Queue 3</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 011 <sub>B</sub> are received on the port.
PQ2	5:4	rw	<b>Priority Queue 2</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 010 <sub>B</sub> are received on the port.
PQ1	3:2	rw	<b>Priority Queue 1</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 001 <sub>B</sub> are received on the port.
PQ0	1:0	rw	<b>Priority Queue 0</b> These 2 bits are used as the priority queue when the tagged packets with the user priority = 000 <sub>B</sub> are received on the port.

TOS Priority Map Register

TPM Offset Reset Value  
TOS Priority Map Register 0F<sub>H</sub> FA50<sub>H</sub>



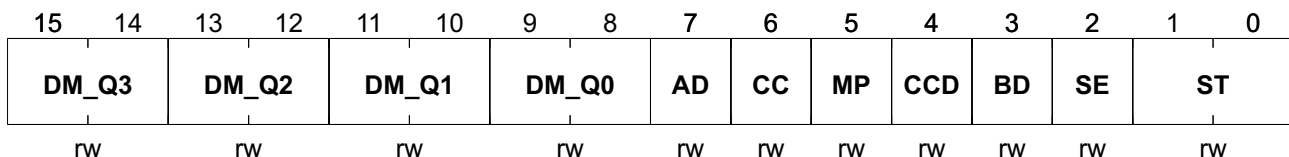
Field	Bits	Type	Description
PQ7	15:14	rw	<b>Priority Queue 7</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 111 <sub>B</sub> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
PQ6	13:12	rw	<b>Priority Queue 6</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 110 <sub>B</sub>
PQ5	11:10	rw	<b>Priority Queue 5</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 101 <sub>B</sub>

Registers Description

Field	Bits	Type	Description
PQ4	9:8	rw	<b>Priority Queue 4</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 100 <sub>B</sub>
PQ3	7:6	rw	<b>Priority Queue 3</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 011 <sub>B</sub>
PQ2	5:4	rw	<b>Priority Queue 2</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 010 <sub>B</sub>
PQ1	3:2	rw	<b>Priority Queue 1</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 001 <sub>B</sub>
PQ0	1:0	rw	<b>Priority Queue 0</b> These 2 bits are used as the priority queue, when the most significant 3 bits in the TOS field are 000 <sub>B</sub>

System Control Register 2

**SC2** **Offset** **Reset Value**  
**System Control Register 2** **10<sub>H</sub>** **0040<sub>H</sub>**



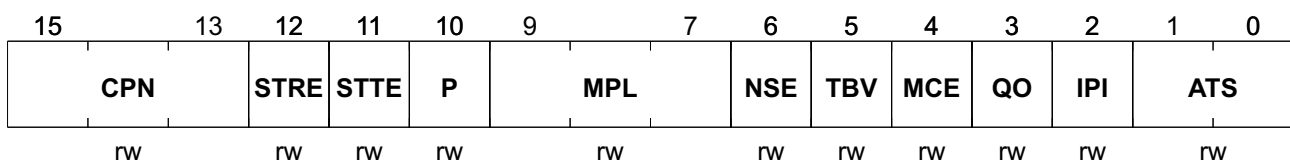
Field	Bits	Type	Description
DM_Q3	15:14	rw	<b>Discard Mode Q3</b> Discard Mode (Drop scheme for Packets Classified as Q3) . See <a href="#">Chapter 3.1.11 Smart Discard</a> for more detail information.
DM_Q2	13:12	rw	<b>Discard Mode Q2</b> Discard Mode (Drop scheme for Packets Classified as Q2) . See <a href="#">Chapter 3.1.11 Smart Discard</a> for more detail information.
DM_Q1	11:10	rw	<b>Discard Mode Q1</b> Discard Mode (Drop scheme for Packets Classified as Q1) . See <a href="#">Chapter 3.1.11 Smart Discard</a> for more detail information.
DM_Q0	9:8	rw	<b>Discard Mode Q0</b> Discard Mode (Drop scheme for Packets Classified as Q0) . See <a href="#">Chapter 3.1.11 Smart Discard</a> for more detail information.
AD	7	rw	<b>Ageing Disable</b> Useless in Samurai-6M/6MX (ADM6996M/MX) 0 <sub>B</sub> Age enabled 1 <sub>B</sub> Age disabled

Registers Description

Field	Bits	Type	Description
CC	6	rw	<b>Rx Clock Change to Tx Clock for GPSI Interface</b> $0_B$ Samurai-6M/6MX (ADM6996M/MX) does not use Tx clock to replace Rx clock when Rx clock stops. $1_B$ Samurai-6M/6MX (ADM6996M/MX) uses Tx clock to replace Rx clock when Rx clock stops
MP	5	rw	<b>Multicast Packet Counted into the Storm Counter</b> $0_B$ Only broadcast packets are counted into the storming counter $1_B$ Multicast and broadcast packets are counted into the storming counter
CCD	4	rw	<b>CRC Check Disable</b> $0_B$ Checks CRC $1_B$ Doesn't check CRC
BD	3	rw	<b>Back Off Disable</b> $0_B$ Back-off is enabled $1_B$ Back-off is disabled
SE	2	rw	<b>Storming Enable</b> It is used in ADM6996L/F style storm control. $0_B$ Disable broadcast/multicast storm protection. $1_B$ Enable broadcast/multicast storm protection.
ST	1:0	rw	<b>Storming Threshold[1:0]</b> It is used in ADM6996L/F style storm control.

System Control Register 3

**SC3** **Offset** **Reset Value**  
**System Control Register 3** **11<sub>H</sub>** **E300<sub>H</sub>**



Field	Bits	Type	Description
CPN	15:13	rw	<b>CPU Port Number</b> $000_B$ The CPU is attached to Port 0 $001_B$ The CPU is attached to Port 1 $010_B$ The CPU is attached to Port 2 $011_B$ The CPU is attached to Port 3 $100_B$ The CPU is attached to Port 4 $101_B$ The CPU is attached to Port 5 $111_B$ No CPU exists

Registers Description

Field	Bits	Type	Description
STRE	12	rw	<b>Special TAG Receive Enable</b> 0 <sub>B</sub> Samurai-6M/6MX (ADM6996M/MX) doesn't identify the Special TAG for the incoming packets 1 <sub>B</sub> Samurai-6M/6MX (ADM6996M/MX) identifies the Special TAG for the incoming packets
STTE	11	rw	<b>Special TAG Transmit Enable</b> 0 <sub>B</sub> Samurai-6M/6MX (ADM6996M/MX) does not insert Special TAG for the packets transmitted to the CPU port 1 <sub>B</sub> Samurai-6M/6MX (ADM6996M/MX) inserts Special TAG for the packets transmitted to the CPU port.
P	10	rw	<b>Pause</b> Also adds Special Tag when Special TAG Transmit is enabled . 0 <sub>B</sub> Does not add Special Tag on the PAUSE packets 1 <sub>B</sub> Adds Special Tag in the PAUSE packets
MPL	9:7	rw	<b>Max Packet Length</b> 000 <sub>B</sub> 1518 bytes 001 <sub>B</sub> 1536 bytes 010 <sub>B</sub> 1664 bytes 110 <sub>B</sub> 1522 bytes x11 <sub>B</sub> 1784 bytes 10x <sub>B</sub> 1784 bytes
NSE	6	rw	<b>New Storming Enable</b> 0 <sub>B</sub> Uses the ADM6996L/F style storming control 1 <sub>B</sub> Uses the Samurai-6M/6MX (ADM6996M/MX) style storming control
TBV	5	rw	<b>Tag Base VLAN</b> 0 <sub>B</sub> Port VLAN 1 <sub>B</sub> Tagged VLAN
MCE	4	rw	<b>MAC Clone Enable</b> 0 <sub>B</sub> MAC Clone is disabled 1 <sub>B</sub> MAC Clone is enabled
QO	3	rw	<b>Queue Option</b> It' s the test for the designer in the queue control.
IPI	2	rw	<b>Interrupt Polarity Inverter</b> 0 <sub>B</sub> The interrupt signal is active pull low 1 <sub>B</sub> The interrupt signal is active pull high
ATS	1:0	rw	<b>Aging Timer Select</b> 00 <sub>B</sub> 300 Seconds 01 <sub>B</sub> 75 Seconds 10 <sub>B</sub> 18 Seconds 11 <sub>B</sub> 1 Second

System Control Register 4

<b>SC4</b>	<b>Offset</b>	<b>Reset Value</b>
<b>System Control Register 4</b>	<b>12<sub>H</sub></b>	<b>3600<sub>H</sub></b>



Registers Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DP	DUP COL <sup>SE</sup> <sub>P</sub>	Res	TLE	Res	Res	O5FL	O4FL	O3FL	PI	O2FL	DUAL*	O1FL	LED*	O0FL	
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DP	15	rw	<b>Drop Packet When Excessive Collision Happen</b> 0 <sub>B</sub> Doesn't drop 1 <sub>B</sub> Drops
DUP_COL_SE P	14	rw	<b>Duplex and Col Separate</b> 0 <sub>B</sub> Indicates the duplex and collision status at the same time 1 <sub>B</sub> Indicates the duplex status only
Res	13:12	rw	<b>Reserved</b>
TLE	11	rw	<b>Ten Limit Enable</b> This function works only when Full Flow Control/Half Back Pressure is enabled. 0 <sub>B</sub> The switch will not ignore 10 Mbit/s paths even when the ten limit reaches 1 <sub>B</sub> The switch will forward packets with Multicast, Broadcast, or Unicast but not learned DA addresses from 100 Mbit/s only to 100 Mbit/s ports and ignore the 10M paths when the ten limit reaches. This function allows the switch to balance the high and the low speed
Res	10	rw	<b>Reserved</b>
Res	9	rw	<b>Reserved</b>
O5FL	8	rw	<b>OLD P5 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled
O4FL	7	rw	<b>OLD P4 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled
O3FL	6	rw	<b>OLD P3 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled
PI	5	rw	<b>Pause Ignore</b> 0 <sub>B</sub> Doesn't ignore Pause packets 1 <sub>B</sub> Ignores Pause packets in half duplex or in full duplex when flow control is not enabled
O2FL	4	rw	<b>OLD P2 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled
DUAL- COLOR-EE	3	rw	<b>Dual Color in MDC / MDIO with CPU</b> See <a href="#">Chapter 3.1.12 LED Display</a> for more detailed information. 0 <sub>B</sub> Single Color 1 <sub>B</sub> Dual Color

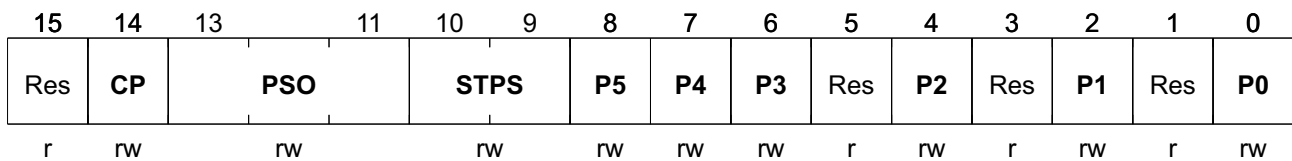
Registers Description

Field	Bits	Type	Description
O1FL	2	rw	<b>OLD P1 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled
LED-ENABLE	1	rw	<b>LED Enable</b> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
O0FL	0	rw	<b>OLD P0 First Lock</b> 0 <sub>B</sub> First Lock is disabled 1 <sub>B</sub> First Lock is enabled

**Port 0 Security Option**

Port Spanning Tree State and Forward Group Port Map.

**P0SO** **Offset**  
**Port 0 Security Option** **13<sub>H</sub>** **Reset Value**  
**01D5<sub>H</sub>**



Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
CP	14	rw	<b>Close Port</b> 0 <sub>B</sub> Doesn't close the port 1 <sub>B</sub> When port security exists, the port is closed automatically
PSO	13:11	rw	<b>Port Security Option</b> 001 <sub>B</sub> Unknown to CPU 010 <sub>B</sub> Discard Unknown 011 <sub>B</sub> First Lock 100 <sub>B</sub> First Link Lock 101 <sub>B</sub> Assign Lock 110 <sub>B</sub> Assign Link Lock

Registers Description

Field	Bits	Type	Description
STPS	10:9	rw	<p><b>Spanning Tree Port Status</b> The Samurai-6M/6MX (ADM6996M/MX) supports 4 port status to support Spanning Tree Protocol .</p> <p>00<sub>B</sub> Forwarding State. The port acts as the normal mode</p> <p>01<sub>B</sub> Disabled State . The port entity will not transmit and receive any packets. Learning is disabled in this state</p> <p>10<sub>B</sub> Learning State . The port entity will only transmit and receive span packets. All other packets are discarded. Learning is enabled for all good frames</p> <p>11<sub>B</sub> Blocking/Listening. Only the span packets defined by Samurai-6M/6MX (ADM6996M/MX) will be received and transmitted. All other packets are discarded by the port entity. Learning is disabled in this state</p>
P5	8	rw	<p><b>Port 5 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 5 is not a member</p> <p>1<sub>B</sub> Port 5 is a member</p>
P4	7	rw	<p><b>Port 4 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 4 is not a member</p> <p>1<sub>B</sub> Port 4 is a member</p>
P3	6	rw	<p><b>Port 3 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 3 is not a member</p> <p>1<sub>B</sub> Port 3 is a member</p>
Res	5	r	<b>Reserved</b>
P2	4	rw	<p><b>Port 2 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 2 is not a member</p> <p>1<sub>B</sub> Port 2 is a member</p>
Res	3	r	<b>Reserved</b>
P1	2	rw	<p><b>Port 1 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 1 is not a member</p> <p>1<sub>B</sub> Port 1 is a member</p>
Res	1	r	<b>Reserved</b>
P0	0	rw	<p><b>Port 0 is a Member of the Forwarding Group</b></p> <p>0<sub>B</sub> Port 0 is not a member</p> <p>1<sub>B</sub> Port 0 is a member</p>

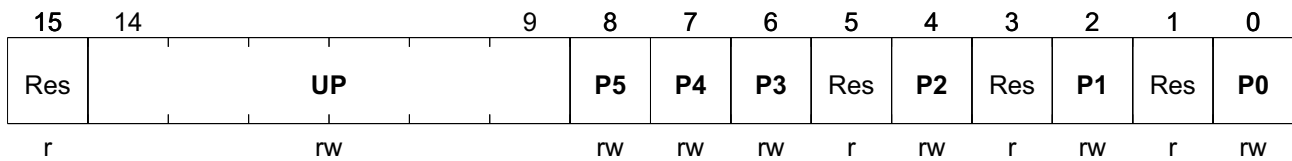
Similar Registers

Table 57 PxSO Registers

Register Short Name	Register Long Name	Offset Address	Page Number
P1SO	Port 1 Security Option	14 <sub>H</sub>	
P2SO	Port 2 Security Option	15 <sub>H</sub>	
P3SO	Port 3 Security Option	16 <sub>H</sub>	
P4SO	Port 4 Security Option	17 <sub>H</sub>	
P5SO	Port 5 Security Option	18 <sub>H</sub>	

**Unicast Port Map and Forward Group Port Map**

**UFGPM** **Offset**  
**Unicast Port Map and Forward Group Port Map** **19<sub>H</sub>** **Reset Value**  
**FFD5<sub>H</sub>**

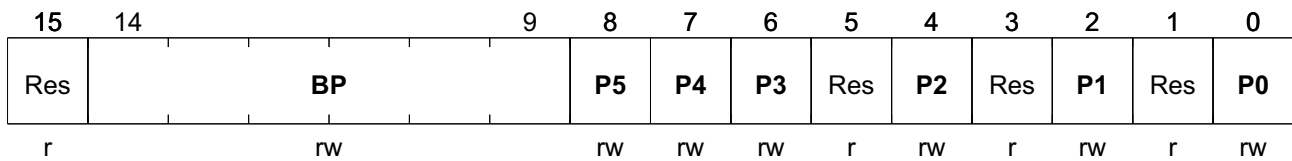


Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
UP	14:9	rw	<b>Unicast Portmap</b> See <a href="#">Chapter 3.1.20 Packet Forwarding</a> for more detailed information.
P5	8	rw	<b>Port 5 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

**Broadcast Port Map and Forward Group Port Map**

**BFGPM** **Offset**  
**Broadcast Port Map and Forward Group Port Map** **1A<sub>H</sub>** **Reset Value**  
**FFD5<sub>H</sub>**

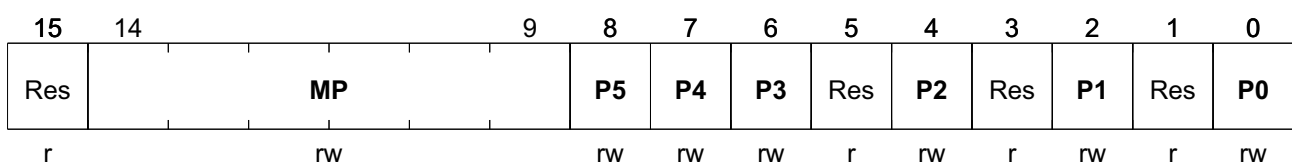
Registers Description



Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
BP	14:9	rw	<b>Broadcast Portmap</b> See <a href="#">Chapter 3.1.20 Packet Forwarding</a> for more detailed information.
P5	8	rw	<b>Port 5 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a Member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

**Multicast Port Map and Forward Group Port Map**

<b>MFGPM</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Multicast Port Map and Forward Group Port Map</b>	<b>1B<sub>H</sub></b>	<b>FFD5<sub>H</sub></b>





Registers Description

Field	Bits	Type	Description
P5	8	rw	<b>Port 5 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

Packet Identification Option, Forward Group Port Map

<b>PIOFGPM</b>	<b>Offset</b>	<b>Reset Value</b>
Packet Identification Option, Forward Group Port Map	1D <sub>H</sub>	FFD5 <sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>MSPH</b>	<b>DIVS</b>	<b>DII6P</b>	<b>DIIPS</b>	<b>DIE</b>	<b>DIIP</b>	<b>DIS</b>	<b>P5</b>	<b>P4</b>	<b>P3</b>	Res	<b>P2</b>	Res	<b>P1</b>	Res	<b>P0</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	r	rw	r	rw

Field	Bits	Type	Description
MSPH	15	rw	<b>MLD Snooping Protocol Header</b> 0 <sub>B</sub> Protocol Header is 01 <sub>H</sub> . 1 <sub>B</sub> Protocol Header is 3A <sub>H</sub> .
DIVS	14	rw	<b>Do not Identify VLAN after SNAP</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify
DII6P	13	rw	<b>Do not Identify IPV6 in PPPOE</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify

Registers Description

Field	Bits	Type	Description
DIIPS	12	rw	<b>Do not Identify IP in PPPOE after SNAP</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify
DIE	11	rw	<b>Do not Identify Ether-Type = 0x0800, IP VER = 6 as IPV6 packets</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify
DIIP	10	rw	<b>Do not Identify IP in PPPOE</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify
DIS	9	rw	<b>Do not Identify SNAP</b> 0 <sub>B</sub> Identify 1 <sub>B</sub> Don't identify
P5	8	rw	<b>Port 5 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

**VLAN Priority Enable and Forward Group Port Map**

**VPEFGPM** Offset **Reset Value**  
**VLAN Priority Enable and Forward Group** **1E<sub>H</sub>** **FFD5<sub>H</sub>**  
**Port Map**

15	14				9	8	7	6	5	4	3	2	1	0
Res		<b>VPE</b>				<b>P5</b>	<b>P4</b>	<b>P3</b>	Res	<b>P2</b>	Res	<b>P1</b>	Res	<b>P0</b>
r		rw				rw	rw	rw	r	rw	r	rw	r	rw



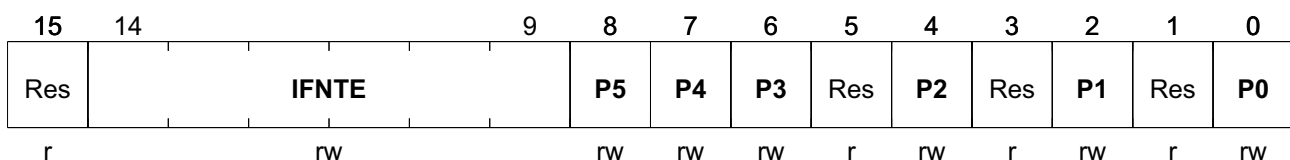


Registers Description

Field	Bits	Type	Description
SPE	14:9	rw	<b>Service Priority Enable</b> 0 <sub>B</sub> Don't care IPV4 TOS /IPV6 Traffic Class 1 <sub>B</sub> Care IPV4 TOS/IPV6 Traffic for priority decision
P5	8	rw	<b>Port 5 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

Input Force No Tag and Forward Group Port Map

**IFNTFGPM** **Offset**  
**Input Force No Tag and Forward Group Port** **20<sub>H</sub>**  
**Map** **Reset Value**  
**FFD5<sub>H</sub>**



Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
IFNTE	14:9	rw	<b>Input Force No TAG Enable</b> 0 <sub>B</sub> Disabled 1 <sub>B</sub> Enabled

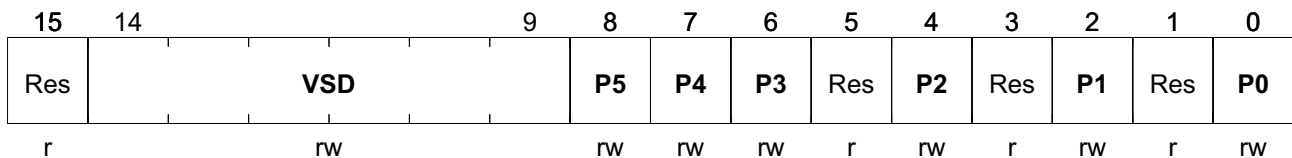


Registers Description

Field	Bits	Type	Description
P3	6	rw	<b>Port 3 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>
P2	4	rw	<b>Port 2 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

VLAN Security Disable and Forward Group Port Map

VSDFGPM	Offset	Reset Value
VLAN Security Disable and Forward Group Port Map	22 <sub>H</sub>	FFD5 <sub>H</sub>



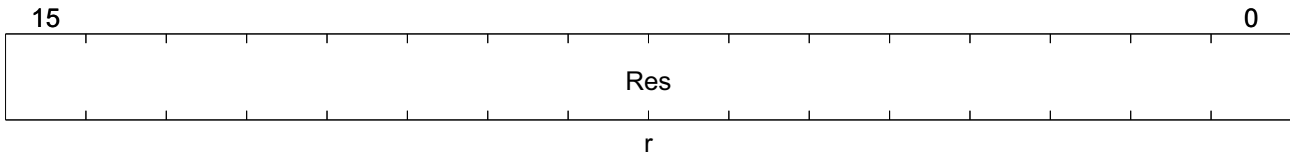
Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
VSD	14:9	rw	<b>VLAN Security Disable</b> 0 <sub>B</sub> Do not disable 1 <sub>B</sub> Disable
P5	8	rw	<b>Port 5 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 5 is not a member 1 <sub>B</sub> Port 5 is a member
P4	7	rw	<b>Port 4 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 4 is not a member 1 <sub>B</sub> Port 4 is a member
P3	6	rw	<b>Port 3 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 3 is not a member 1 <sub>B</sub> Port 3 is a member
Res	5	r	<b>Reserved</b>

Registers Description

Field	Bits	Type	Description
P2	4	rw	<b>Port 2 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 2 is not a member 1 <sub>B</sub> Port 2 is a member
Res	3	r	<b>Reserved</b>
P1	2	rw	<b>Port 1 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 1 is not a member 1 <sub>B</sub> Port 1 is a member
Res	1	r	<b>Reserved</b>
P0	0	rw	<b>Port 0 is a member of the Forwarding Group</b> 0 <sub>B</sub> Port 0 is not a member 1 <sub>B</sub> Port 0 is a member

**Buffer Threshold Register 0**

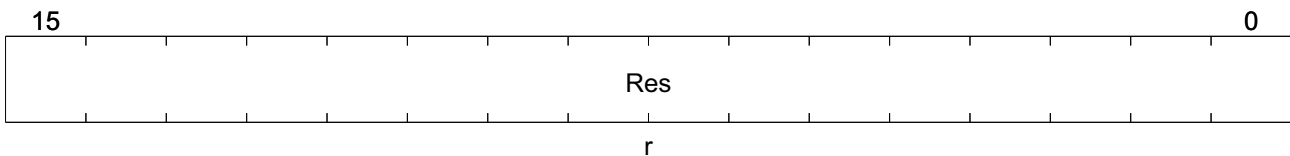
**BT0** **Offset** **Reset Value**  
**Buffer Threshold Register 0** **23<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
Res	15:0	r	Reserved

**Buffer Threshold Register 1**

**BT1** **Offset** **Reset Value**  
**Buffer Threshold Register 1** **24<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
Res	15:0	r	Reserved

**IGMP/MLDTRAP Enable and Input Jam Threshold Register**

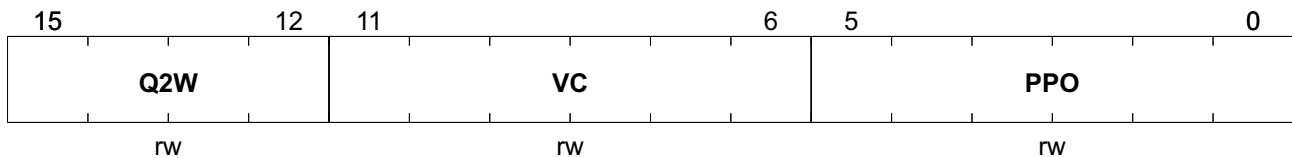
**IMEIJT** **Offset** **Reset Value**  
**IGMP/MLDTRAP Enable and Input Jam** **25<sub>H</sub>** **1000<sub>H</sub>**  
**Threshold Register**



Field	Bits	Type	Description
Q1W	15:12	rw	<b>Queue 1 Weight</b> See <a href="#">Chapter 3.1.15 Priority Queue</a> for more detail information.
IMTE	11:6	rw	<b>IGMP/MLD Trap Enable</b> It is a per port function. 0 <sub>B</sub> The port does not enable its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useless in this port 1 <sub>B</sub> The port enables its multicast snooping function. Trap MLD_IPV6, MLD_IP and IGMP_IP are useful in this port
IJT	5:0	rw	<b>Input Jam Threshold</b>

**Queue 2 Weight, VID Exist Check, and PPPOE Port Only**

Q2WVECPO	Offset	Reset Value
Queue 2 Weight, VID Exist Check, and PPPOE Port Only	26 <sub>H</sub>	1000 <sub>H</sub>

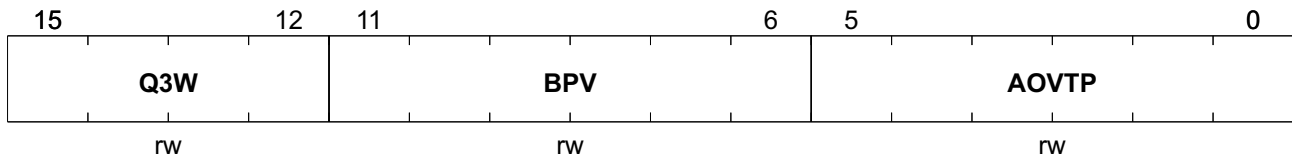


Field	Bits	Type	Description
Q2W	15:12	rw	<b>Queue 2 Weight</b> See <a href="#">Chapter 3.1.15 Priority Queue</a> for more detail information.
VC	11:6	rw	<b>VID Check</b> It is a per port function. 0 <sub>B</sub> Doesn't check 1 <sub>B</sub> checks
PPO	5:0	rw	<b>PPPOE Port Only</b> It's a per port function 0 <sub>B</sub> The port is not a PPPOE Only port 1 <sub>B</sub> The port is a PPPOE Only port

**Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged**

Q3WBPVAO	Offset	Reset Value
Queue 3 Weight, Back to Port VLAN, and Admit Only VLAN-Tagged	27 <sub>H</sub>	1000 <sub>H</sub>

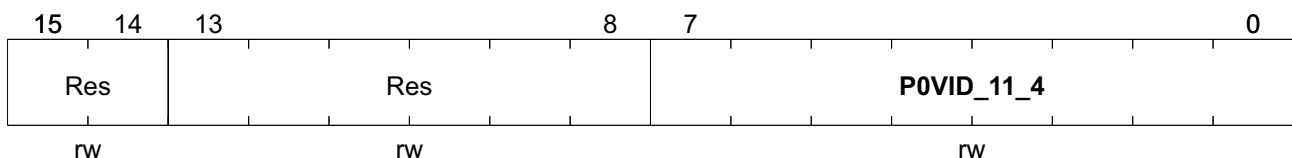
Registers Description



Field	Bits	Type	Description
Q3W	15:12	rw	<b>Queue 3 Weight</b> See <a href="#">Chapter 3.1.15 Priority Queue</a> for more detail information.
BPV	11:6	rw	<b>Back To Port VLAN</b> It is a per port function 0 <sub>B</sub> Doesn't back to Port VLAN 1 <sub>B</sub> Backs to Port VLAN
AOVTP	5:0	rw	<b>Admit Only VLAN_Tagged Packet</b> It is a per port function 0 <sub>B</sub> The port doesn't check if the packets are VLAN-Tagged 1 <sub>B</sub> The port drops the packets that carry no VID. (That is Untagged Packets or Priority-Tagged Packets)

Input Double Tag Enable, and P0VID[11:4]

IDTEP	Offset	Reset Value
Input Double Tag Enable, and P0VID[11:4]	28 <sub>H</sub>	0000 <sub>H</sub>



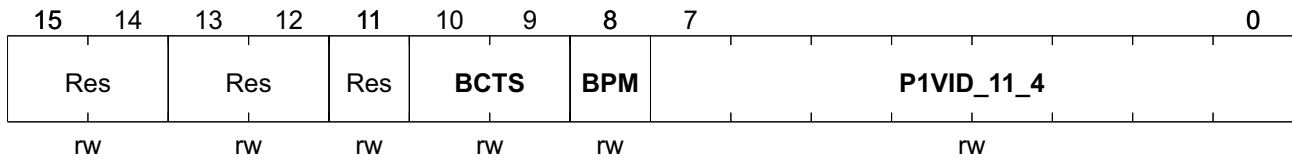
Field	Bits	Type	Description
Res	15:14	rw	<b>Reserved</b>
Res	13:8	rw	<b>Reserved</b>
P0VID_11_4	7:0	rw	<b>P0VID[11:4]</b> VID bit 11 ~ 4 fo Port 0

Output Double Tag Enable, and P1VID[11:4]

ODTEP	Offset	Reset Value
Output Double Tag Enable, and P1VID[11:4]	29 <sub>H</sub>	0000 <sub>H</sub>



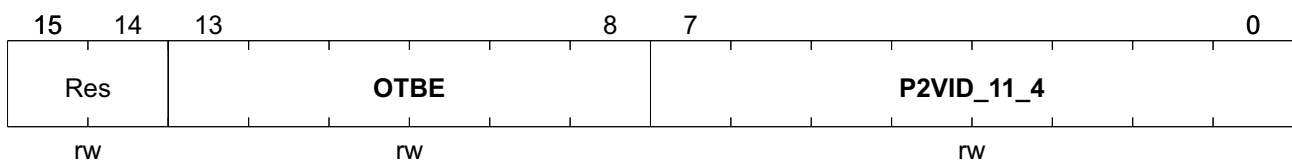
Registers Description



Field	Bits	Type	Description
Res	15:14	rw	<b>Reserved</b>
Res	13:12	rw	<b>Reserved</b>
Res	11	rw	<b>Reserved</b>
BCTS	10:9	rw	<b>Bandwidth Control Timer Select</b> 00 <sub>B</sub> 8 ms, 64Kbps step, apply to 64Kbps~2.2Mbps 01 <sub>B</sub> 1 ms, 512Kbps step, apply to 512Kbps~18Mbps 10 <sub>B</sub> 40 us, 200Kbps step, apply to 200Kbps~100Mbps 11 <sub>B</sub> 500 us, 16Kbps step, apply to 16Kbps~32Mbps
BPM	8	rw	<b>Back Pressure Mechanism</b> 0 <sub>B</sub> Exit collision state when CRS goes low 1 <sub>B</sub> Exit collision state when RXDV goes low
P1VID_11_4	7:0	rw	<b>P1VID[11:4]</b> VID bit 11 ~ 4 of Port 1.

**Output Tag Bypass, and P2VID[11:4]**

<b>OTBP</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Output Tag Bypass, and P2VID[11:4]</b>	<b>2A<sub>H</sub></b>	<b>3F00<sub>H</sub></b>

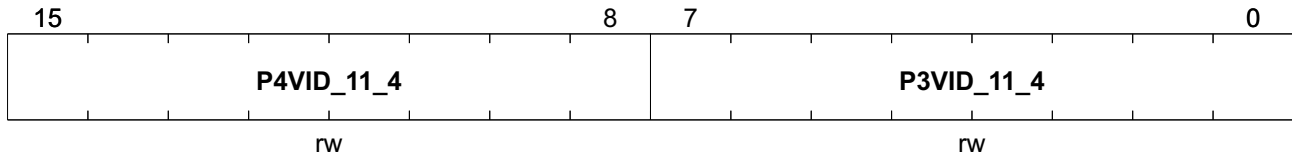


Field	Bits	Type	Description
Res	15:14	rw	<b>Reserved</b>
OTBE	13:8	rw	<b>Output Tag Bypass Enable</b> It's a per port function. See <a href="#">Chapter 3.1.14.12 Egress Tag Rule</a> for more detailed information.
P2VID_11_4	7:0	rw	<b>P2VID[11:4]</b> VID bit 11 ~ 4 of Port 2.

**P3VID[11:4], and P4VID[11:4]**

Registers Description

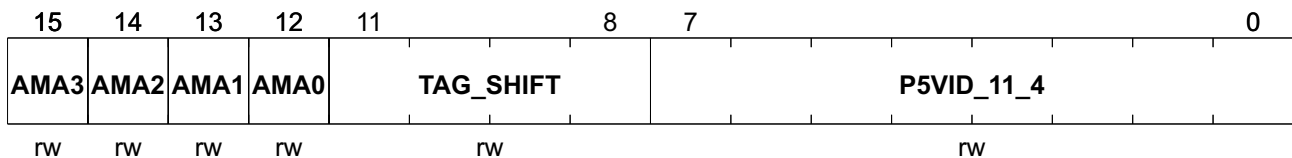
**P11\_4** **Offset** **Reset Value**  
**P3VID[11:4], and P4VID[11:4]** **2B<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
P4VID_11_4	15:8	rw	<b>P4VID[11:4]</b> VID bit 11 ~ 4 of Port 4.
P3VID_11_4	7:0	rw	<b>P3VID[11:4]</b> VID bit 11 ~ 4 of Port 3.

**Reserved Address Control, and P5VID[11:4]**

**RACP** **Offset** **Reset Value**  
**Reserved Address Control, and P5VID[11:4]** **2C<sub>H</sub>** **D000<sub>H</sub>**

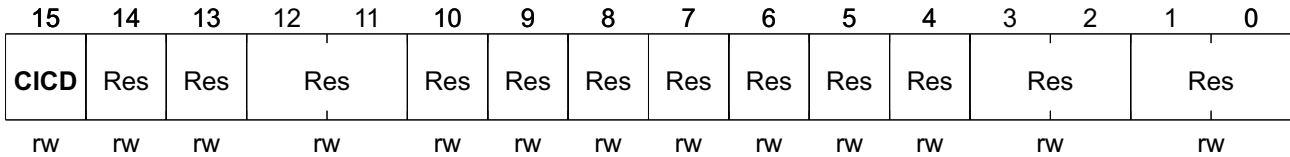


Field	Bits	Type	Description
AMA3	15	rw	<b>Action of MAC Address 3</b> The Action of MAC Address = 0180C2000010 <sub>H</sub> ~ 0180C20000FF <sub>H</sub>
AMA2	14	rw	<b>Action of MAC Address 2</b> The Action of MAC Address = 0180C2000002 <sub>H</sub> ~ 0180C200000F <sub>H</sub>
AMA1	13	rw	<b>Action of MAC Address 1</b> The Action of MAC Address = 0180C2000001 <sub>H</sub>
AMA0	12	rw	<b>Action of MAC Address 0</b> The Action of MAC Address = 0180C2000000 <sub>H</sub>
TAG_SHIFT	11:8	rw	<b>Tag Shift</b>
P5VID_11_4	7:0	rw	<b>P5VID[11:4]</b> VID bit 11 ~ 4 of Port 5

**PHY Control Register**

Registers Description

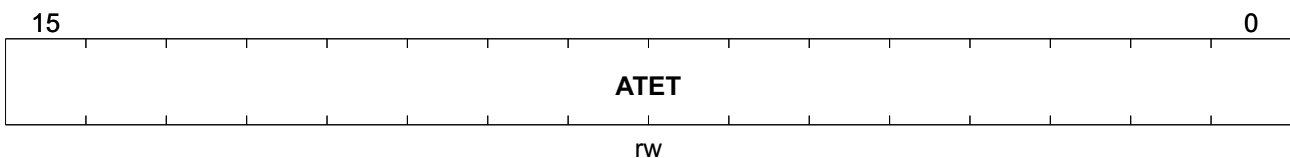
**PHYC** **Offset** **Reset Value**  
**PHY Control Register** **2D<sub>H</sub>** **4442<sub>H</sub>**



Field	Bits	Type	Description
CICD	15	rw	<b>Chip ID Check Disable</b> 0 <sub>B</sub> Checks CHIP ID in 32 bit SDC/SDO 1 <sub>B</sub> Doesn't check CHIP ID in 32 bit SDC/SDIO
Res	14	rw	<b>Reserved</b>
Res	13	rw	<b>Reserved</b>
Res	12:11	rw	<b>Reserved</b>
Res	10	rw	<b>Reserved</b>
Res	9	rw	<b>Reserved</b>
Res	8	rw	<b>Reserved</b>
Res	7	rw	<b>Reserved</b>
Res	6	rw	<b>Reserved</b>
Res	5	rw	<b>Reserved</b>
Res	4	rw	<b>Reserved</b>
Res	3:2	rw	<b>Reserved</b>
Res	1:0	rw	<b>Reserved</b>

**ADM TAG Ether Type**

**ATET** **Offset** **Reset Value**  
**ADM TAG Ether Type** **2E<sub>H</sub>** **0000<sub>H</sub>**

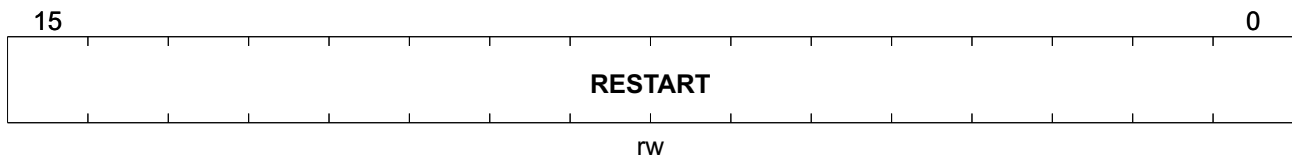


Registers Description

Field	Bits	Type	Description
ATET	15:0	rw	<b>ADM TAG Ether Type</b> This value is used by the user to define their Ether-Type. When Special Tag Receive is enabled, Samurai-6M/6MX (ADM6996M/MX) checks the packets on the CPU port to see if the two bytes following the SA are the same as ADM TAG Ether Type . If they are different, Samurai-6M/6MX (ADM6996M/MX) bypasses the Special Tag. If the same, Samurai-6M/6MX (ADM6996M/MX) will use the value in the Special Tag to do switching decisions .

**PHY Restart Register**

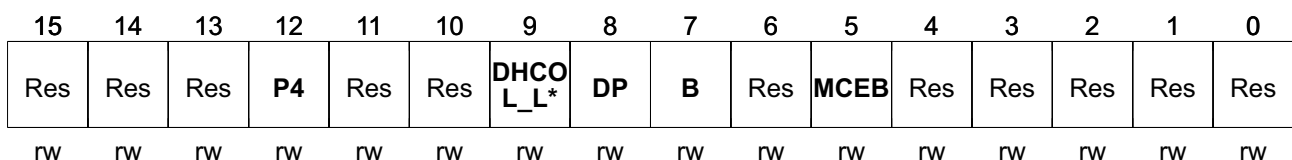
**PR** **Offset**  
**PHY Restart Register** **2F<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
RESTART	15:0	rw	<b>Restart</b> Samurai-6M/6MX (ADM6996M/MX) writes this register to restart all the PHYs in the switch. The value written is not important.

**Miscellaneous Register**

**MISC** **Offset**  
**Miscellaneous Register** **30<sub>H</sub>** **Reset Value**  
**0987<sub>H</sub>**



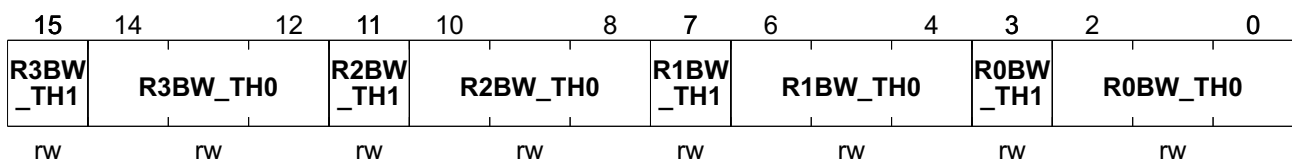
Field	Bits	Type	Description
Res	15	rw	<b>Reserved</b>
Res	14	rw	<b>Reserved</b>
Res	13	rw	<b>Reserved</b>

Registers Description

Field	Bits	Type	Description
P4	12	rw	<b>Port 4 LED Mode</b> 0 <sub>B</sub> LinkAct/DupCol/Speed. 1 <sub>B</sub> Link/Act/Speed.
Res	11	rw	<b>Reserved</b>
Res	10	rw	<b>Reserved</b>
DHCOL_LED_EN	9	rw	<b>Dual Speed Hub COL_LED Enable</b> 0 <sub>B</sub> Normal LED display. 1 <sub>B</sub> Dual Speed Hub LED display. Port0 Col LED: 10M Col LED. Port1 Col LED: 100M Col LED.
DP	8	rw	<b>Drop Packets</b> Drop packets when the link partner does not follow the PAUSE protocol. 0 <sub>B</sub> Disable. 1 <sub>B</sub> Enable to drop packets.
B	7	rw	<b>BYPASS</b> Bypass Tag/Untag function. 0 <sub>B</sub> Disable. 1 <sub>B</sub> Enable to bypass Tag/Untag function
Res	6	rw	<b>Reserved</b>
MCEB	5	rw	<b>MAC Clone Enable Bits Select</b> 0 <sub>B</sub> Select 1 bit MAC Clone function. 1 <sub>B</sub> Select 2 bits MAC Clone function.
Res	4	rw	<b>Reserved</b>
Res	3	rw	<b>Reserved</b>
Res	2	rw	<b>Reserved</b>
Res	1	rw	<b>Reserved</b>
Res	0	rw	<b>Reserved</b>

**Basic Bandwidth Control Register 0**

**BBC0** **Offset** **Reset Value**  
**Basic Bandwidth Control Register 0** **31<sub>H</sub>** **0000<sub>H</sub>**



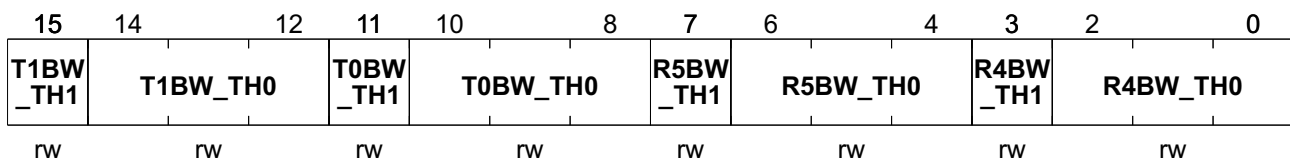
Field	Bits	Type	Description
R3BW_TH1	15	rw	<b>Port 3 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P3RBCE</a> for more details.
R3BW_TH0	14:12	rw	<b>Port 3 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P3RBCE</a> for more details.

Registers Description

Field	Bits	Type	Description
R2BW_TH1	11	rw	<b>Port 2 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P2RBCE</a> for more details.
R2BW_TH0	10:8	rw	<b>Port 2 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P2RBCE</a> for more details.
R1BW_TH1	7	rw	<b>Port 1 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P1RBCE</a> for more details.
R1BW_TH0	6:4	rw	<b>Port 1 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P1RBCE</a> for more details.
R0BW_TH1	3	rw	<b>Port 0 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P0RBCE</a> for more details.
R0BW_TH0	2:0	rw	<b>Port 0 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P0RBCE</a> for more details.

**Basic Bandwidth Control Register 1**

<b>BBC1</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Basic Bandwidth Control Register 1</b>	<b>32<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
T1BW_TH1	15	rw	<b>Port 1 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P1TBCE</a> for more details.
T1BW_TH0	14:12	rw	<b>Port 1 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <a href="#">P1TBCE</a> for more details.
T0BW_TH1	11	rw	<b>Port 0 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P0TBCE</a> for more details.
T0BW_TH0	10:8	rw	<b>Port 0 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <a href="#">P0TBCE</a> for more details.
R5BW_TH1	7	rw	<b>Port 5 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P5RBCE</a> for more details.
R5BW_TH0	6:4	rw	<b>Port 5 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P5RBCE</a> for more details.
R4BW_TH1	3	rw	<b>Port 4 Receive Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <a href="#">P4RBCE</a> for more details.
R4BW_TH0	2:0	rw	<b>Port 4 Receive Bandwidth Configuration</b> See register 0033 <sub>H</sub> , <a href="#">P4RBCE</a> for more details.

**Bandwidth Control Enable Register**

**BCE** **Offset** **Reset Value**  
**Bandwidth Control Enable Register** **33<sub>H</sub>** **0000<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>IPCP</b>	<b>CLC</b>	Res	<b>ANBCE</b>	<b>P5TBCE</b>	<b>P4TBCE</b>	<b>P3TBCE</b>	<b>P5RBCE</b>	<b>P4RBCE</b>	<b>P3RBCE</b>	<b>P2TBCE</b>	<b>P2RBCE</b>	<b>P1TBCE</b>	<b>P1RBCE</b>	<b>P0TBCE</b>	<b>P0RBCE</b>
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IPCP	15	rw	<b>Invert P4 Clock in PCS</b> 0 <sub>D</sub> Disable 1 <sub>D</sub> Enable
CLC	14	rw	<b>Check the Length of CRS</b> 0 <sub>D</sub> Enable 1 <sub>D</sub> Disable
Res	13	rw	<b>Reserved</b>
ANBCE	12	rw	<b>Samurai-6M/6MX (ADM6996M/MX) New Bandwidth Control Enable</b> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P5TBCE	11	rw	<b>Port 5 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T5BW_TH3</b> , <b>T5BW_TH2</b> , <b>T5BW_TH1</b> , <b>T5BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P4TBCE	10	rw	<b>Port 4 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T4BW_TH3</b> , <b>T4BW_TH2</b> , <b>T4BW_TH1</b> , <b>T4BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P3TBCE	9	rw	<b>Port 3 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T3BW_TH3</b> , <b>T3BW_TH2</b> , <b>T3BW_TH1</b> , <b>T3BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P5RBCE	8	rw	<b>Port 5 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R5BW_TH3</b> , <b>R5BW_TH2</b> , <b>R5BW_TH1</b> , <b>R5BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable

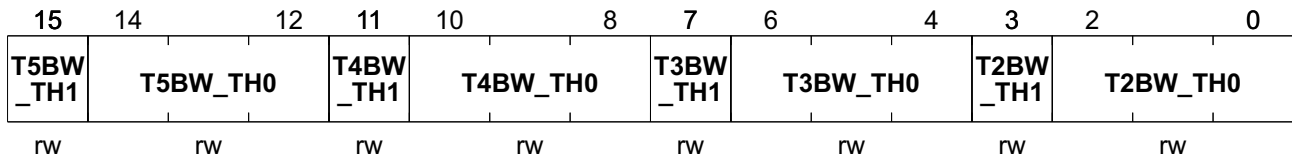
Field	Bits	Type	Description
P4RBCE	7	rw	<b>Port 4 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R4BW_TH3, R4BW_TH2, R4BW_TH1, R4BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P3RBCE	6	rw	<b>Port 3 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R3BW_TH3, R3BW_TH2, R3BW_TH1, R3BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P2TBCE	5	rw	<b>Port 2 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T2BW_TH3, T2BW_TH2, T2BW_TH1, T2BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P2RBCE	4	rw	<b>Port 2 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R2BW_TH3, R2BW_TH2, R2BW_TH1, R2BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P1TBCE	3	rw	<b>Port 1 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T1BW_TH3, T1BW_TH2, T1BW_TH1, T1BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P1RBCE	2	rw	<b>Port 1 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R1BW_TH3, R1BW_TH2, R1BW_TH1, R1BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P0TBCE	1	rw	<b>Port 0 Transmit Bandwidth Control Enable</b> The transmitted bandwidth is { <b>T0BW_TH3, T0BW_TH2, T0BW_TH1, T0BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
P0RBCE	0	rw	<b>Port 0 Receive Bandwidth Control Enable</b> The received bandwidth is { <b>R0BW_TH3, R0BW_TH2, R0BW_TH1, R0BW_TH0</b> , 000000 <sub>B</sub> } kbit/s. K = 1000. 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable

#### Extended Bandwidth Control Register 0

EBC0	Offset	Reset Value
Extended Bandwidth Control Register 0	34 <sub>H</sub>	0000 <sub>H</sub>



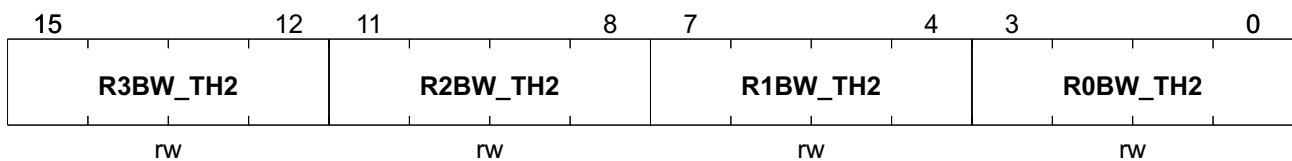
Registers Description



Field	Bits	Type	Description
T5BW_TH1	15	rw	<b>Port 5 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <b>P5TBCE</b> for more details.
T5BW_TH0	14:12	rw	<b>Port 5 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <b>P5TBCE</b> for more details.
T4BW_TH1	11	rw	<b>Port 4 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <b>P4TBCE</b> for more details.
T4BW_TH0	10:8	rw	<b>Port 4 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <b>P4TBCE</b> for more details.
T3BW_TH1	7	rw	<b>Port 3 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <b>P3TBCE</b> for more details.
T3BW_TH0	6:4	rw	<b>Port 3 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <b>P3TBCE</b> for more details.
T2BW_TH1	3	rw	<b>Port 2 Transmit Bandwidth Maximum[3].</b> See register 0033 <sub>H</sub> , <b>P2TBCE</b> for more details.
T2BW_TH0	2:0	rw	<b>Port 2 Transmit Bandwidth Maximum[2:0].</b> See register 0033 <sub>H</sub> , <b>P2TBCE</b> for more details.

Extended Bandwidth Control Register 1

<b>EBC1</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Extended Bandwidth Control Register 1</b>	<b>35<sub>H</sub></b>	<b>0000<sub>H</sub></b>



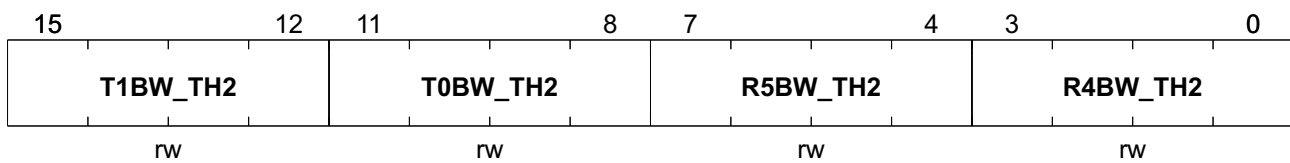
Field	Bits	Type	Description
R3BW_TH2	15:12	rw	<b>Port 3 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P3RBCE</b> for more details.
R2BW_TH2	11:8	rw	<b>Port 2 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P2RBCE</b> for more details.
R1BW_TH2	7:4	rw	<b>Port 1 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P1RBCE</b> for more details.

Registers Description

Field	Bits	Type	Description
R0BW_TH2	3:0	rw	<b>Port 0 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P0RBCE</b> for more details.

**Extended Bandwidth Control Register 2**

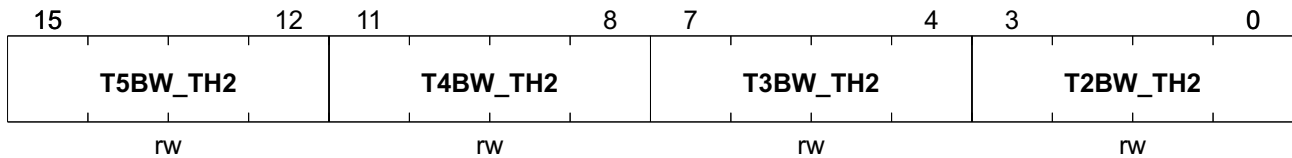
<b>EBC2</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Extended Bandwidth Control Register 2</b>	<b>36<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
T1BW_TH2	15:12	rw	<b>Port 1 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P1TBCE</b> for more details.
T0BW_TH2	11:8	rw	<b>Port 0 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P0TBCE</b> for more details.
R5BW_TH2	7:4	rw	<b>Port 5 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P5RBCE</b> for more details.
R4BW_TH2	3:0	rw	<b>Port 4 Receive Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <b>P4RBCE</b> for more details.

### Extended Bandwidth Control Register 3

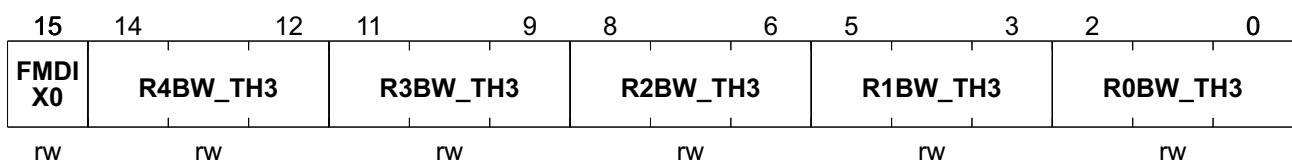
**EBC3** **Offset**  
**Extended Bandwidth Control Register 3** **37<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
T5BW_TH2	15:12	rw	<b>Port 5 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <a href="#">P5TBCE</a> for more details.
T4BW_TH2	11:8	rw	<b>Port 4 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <a href="#">P4TBCE</a> for more details.
T3BW_TH2	7:4	rw	<b>Port 3 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <a href="#">P3TBCE</a> for more details.
T2BW_TH2	3:0	rw	<b>Port 2 Transmit Bandwidth Maximum[7:4].</b> See register 0033 <sub>H</sub> , <a href="#">P2TBCE</a> for more details.

### Extended Bandwidth Control Register 4

**EBC4** **Offset**  
**Extended Bandwidth Control Register 4** **38<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



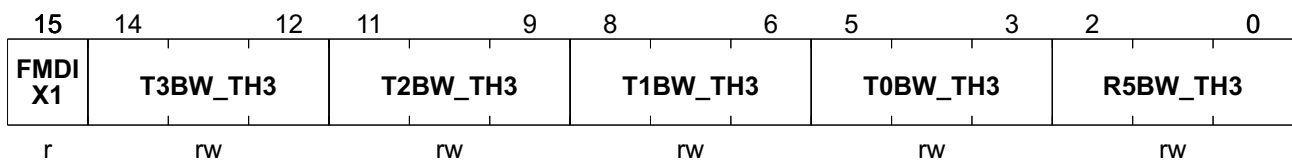
Field	Bits	Type	Description
FMDIX0	15	rw	<b>Port 0 MDIX Control</b> This bit can be used for Port 0 MDI/MDIX selection. It is useful when Port 0 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 <sub>B</sub> Using MDI 1 <sub>B</sub> Using MDIX
R4BW_TH3	14:12	rw	<b>Port 4 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P4RBCE</a> for more details.

Registers Description

Field	Bits	Type	Description
R3BW_TH3	11:9	rw	<b>Port 3 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P3RBCE</a> for more details.
R2BW_TH3	8:6	rw	<b>Port 2 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P2RBCE</a> for more details.
R1BW_TH3	5:3	rw	<b>Port 1 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P1RBCE</a> for more details.
R0BW_TH3	2:0	rw	<b>Port 0 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P0RBCE</a> for more details.

**Extended Bandwidth Control Register 5**

<b>EBC5</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Extended Bandwidth Control Register 5</b>	<b>39<sub>H</sub></b>	<b>0000<sub>H</sub></b>

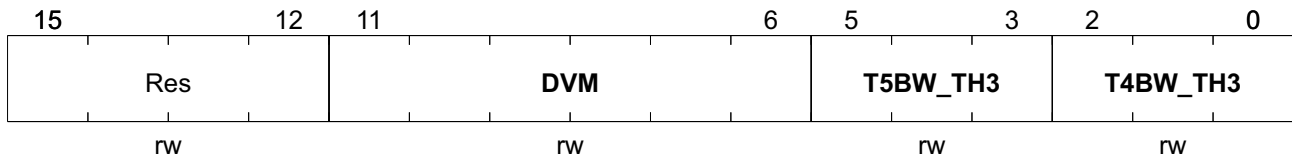


Field	Bits	Type	Description
FMDIX1	15	r	<b>Port 1 MDIX Control</b> This bit can be used for Port 1 MDI/MDIX selection. It is useful when Port 1 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 <sub>B</sub> Using MDI 1 <sub>B</sub> Using MDIX
T3BW_TH3	14:12	rw	<b>Port 3 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P3TBCE</a> for more details.
T2BW_TH3	11:9	rw	<b>Port 2 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P2TBCE</a> for more details.
T1BW_TH3	8:6	rw	<b>Port 1 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P1TBCE</a> for more details.
T0BW_TH3	5:3	rw	<b>Port 0 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P0TBCE</a> for more details.
R5BW_TH3	2:0	rw	<b>Port 5 Receive Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <a href="#">P5RBCE</a> for more details.

**Default VLAN Member and Extended Bandwidth Control Register 6**

Registers Description

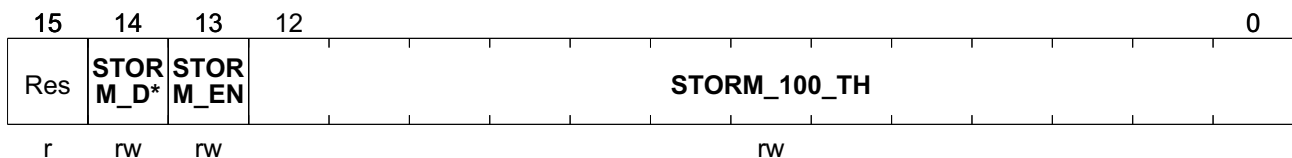
**DVMEBC6** **Offset**  
3A<sub>H</sub> **Reset Value**  
0FC0<sub>H</sub>  
**Default VLAN Member and Extended Bandwidth Control Register 6**



Field	Bits	Type	Description
Res	15:12	rw	<b>Reserved</b>
DVM	11:6	rw	<b>Default VLAN Member</b>
T5BW_TH3	5:3	rw	<b>Port 5 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <b>P5TBCE</b> for more details.
T4BW_TH3	2:0	rw	<b>Port 4 Transmit Bandwidth Maximum[10:8].</b> See register 0033 <sub>H</sub> , <b>P4TBCE</b> for more details.

**New Storm Register 0**

**NS0** **Offset**  
3B<sub>H</sub> **Reset Value**  
0000<sub>H</sub>  
**New Storm Register 0**



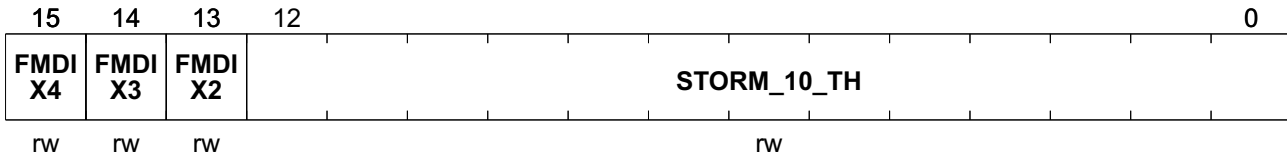
Field	Bits	Type	Description
Res	15	r	<b>Reserved</b>
STORM_DRO P_EN	14	rw	<b>Storm Drop Enable</b> 0 <sub>B</sub> Doesn't drop in the storming period 1 <sub>B</sub> Drops in the storming period
STORM_EN	13	rw	<b>Storm Enable</b> 0 <sub>B</sub> Disable Samurai-6M/6MX (ADM6996M/MX) style broadcast storm protection 1 <sub>B</sub> Enable Samurai-6M/6MX (ADM6996M/MX) style broadcast storm protection

Registers Description

Field	Bits	Type	Description
STORM_100_TH	12:0	rw	<b>100M Threshold</b> See <a href="#">Chapter 3.1.9 Broadcast Storm</a> for more detailed information. It is used when all ports link up in the 100M. The upper bound is reached when the number of the packets received during the 50 ms is over 100M Threshold.

**New Storm Register 1**

**NS1** **Offset** **Reset Value**  
**New Storm Register 1** **3C<sub>H</sub>** **0000<sub>H</sub>**

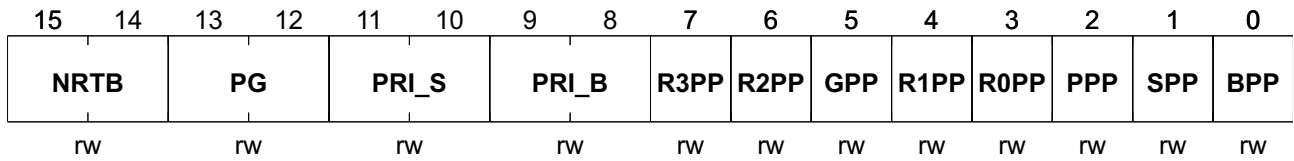


Field	Bits	Type	Description
FMDIX4	15	rw	<b>Port 4 MDIX Control</b> This bit can be used for Port 4 MDI/MDIX selection. It is useful when Port 4 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 <sub>B</sub> Using MDI 1 <sub>B</sub> Using MDIX
FMDIX3	14	rw	<b>Port 3 MDIX Control</b> This bit can be used for Port 3 MDI/MDIX selection. It is useful when Port 3 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 <sub>B</sub> Using MDI 1 <sub>B</sub> Using MDIX
FMDIX2	13	rw	<b>Port 2 MDIX Control</b> This bit can be used for Port 2 MDI/MDIX selection. It is useful when Port 2 Crossover Auto Detect is disabled and 16 bits management interface (SDC/SDIO) is used. 0 <sub>B</sub> Using MDI 1 <sub>B</sub> Using MDIX
STORM_10_TH	12:0	rw	<b>10M Threshold</b> See <a href="#">Chapter 3.1.9 Broadcast Storm</a> for more detailed information. It is used when one of ports link up in the 10M. The upper bound is reached when the number of the packets received during the 50 ms is over 10M Threshold.

**New Reserve Address Control Register 0**

**NRAC0** **Offset** **Reset Value**  
**New Reserve Address Control Register 0** **3D<sub>H</sub>** **00FD<sub>H</sub>**

Registers Description



Field	Bits	Type	Description
NRTB	15:14	rw	<b>New Reserve TXTAG for BPDU</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
PG	13:12	rw	<b>PRI for GXP</b> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
PRI_S	11:10	rw	<b>PRI for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3</b> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
PRI_B	9:8	rw	<b>PRI for BPDU</b> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3
R3PP	7	rw	<b>RESER_R3 Pass Portmap</b> 0 <sub>B</sub> RESER_R3 Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> RESER_R3 Pass Portmap is 111111 <sub>B</sub>
R2PP	6	rw	<b>RESER_R2 Pass Portmap</b> 0 <sub>B</sub> RESER_R2 Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> RESER_R2 Pass Portmap is 111111 <sub>B</sub>
GPP	5	rw	<b>GXP Pass Portmap</b> 0 <sub>B</sub> GXP Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> GXP Pass Portmap is 111111 <sub>B</sub>
R1PP	4	rw	<b>RESER_R1 Pass Portmap</b> 0 <sub>B</sub> RESER_R1 Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> RESER_R1 Pass Portmap is 111111 <sub>B</sub>
R0PP	3	rw	<b>RESER_R0 Pass Portmap</b> 0 <sub>B</sub> RESER_R0 Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> RESER_R0 Pass Portmap is 111111 <sub>B</sub>
PPP	2	rw	<b>PAE Pass Portmap</b> 0 <sub>B</sub> PAE Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> PAE Pass Portmap is 111111 <sub>B</sub>

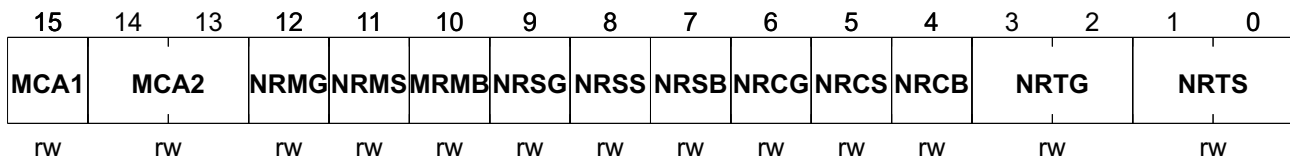


Registers Description

Field	Bits	Type	Description
SPP	1	rw	<b>Slow Pass Portmap</b> 0 <sub>B</sub> SLOW Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> SLOW Pass Portmap is 111111 <sub>B</sub>
BPP	0	rw	<b>BPDU Pass Portmap</b> 0 <sub>B</sub> BPDU Pass Portmap is 000000 <sub>B</sub> 1 <sub>B</sub> BPDU Pass Portmap is 111111 <sub>B</sub>

**New Reserve Address Control Register 1**

**NRAC1** **Offset** **Reset Value**  
**New Reserve Address Control Register 1** **3E<sub>H</sub>** **0000<sub>H</sub>**



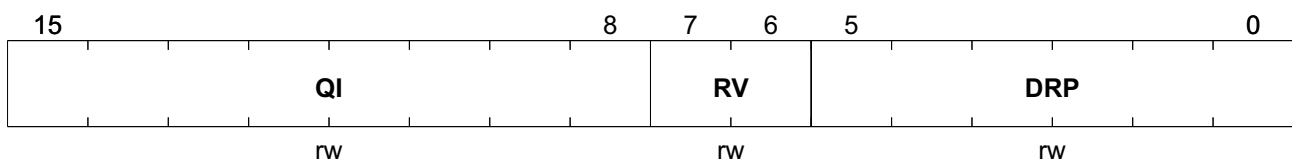
Field	Bits	Type	Description
MCA1	15	rw	<b>Mac Control Action 1</b> Mac Control Action when OPCODE is 01 <sub>H</sub> 0 <sub>B</sub> The same as Mac Control Action when OPCODE is not 01 <sub>H</sub> 1 <sub>B</sub> Discards
MCA2	14:13	rw	<b>Mac Control Action 2</b> Mac Control Action when OPCODE is not 01 <sub>H</sub> 00 <sub>B</sub> Defaults Output Ports 01 <sub>B</sub> Discards 10 <sub>B</sub> If the receiving port is the CPU port, forward it to the default output ports. If the receiving port is not the CPU port, forward it to the CPU port 11 <sub>B</sub> Forwards to the default output ports except the CPU port
NRMG	12	rw	<b>New Reserve Management for GXP</b> 0 <sub>B</sub> Doesn't identify as management packets 1 <sub>B</sub> Identifies as management packets
NRMS	11	rw	<b>New Reserve Management for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3</b> 0 <sub>B</sub> Doesn't identify as management packets 1 <sub>B</sub> Identifies as management packets
MRMB	10	rw	<b>New Reserve Management for BPDU</b> 0 <sub>B</sub> Doesn't identify as management packets 1 <sub>B</sub> Identifies as management packets
NRSB	9	rw	<b>New Reserve Span for GXP</b> 0 <sub>B</sub> Doesn't identify as management packets 1 <sub>B</sub> Identifies as management packets

Registers Description

Field	Bits	Type	Description
NRSS	8	rw	<b>New Reserve Span for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3</b> 0 <sub>B</sub> Doesn't identify as span packets 1 <sub>B</sub> Identifies as span packets
NRSB	7	rw	<b>New Reserve SPAN for BPDU</b> 0 <sub>B</sub> Doesn't identify as span packets 1 <sub>B</sub> Identifies as span packets
NRCG	6	rw	<b>New Reserve Cross_VLAN for GXP</b> 0 <sub>B</sub> Follows VLAN 1 <sub>B</sub> Crosses VLAN
NRCS	5	rw	<b>New Reserve Cross_VLAN. for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3</b> 0 <sub>B</sub> Follows VLAN 1 <sub>B</sub> Crosses VLAN
NRCB	4	rw	<b>New Reserve Cross_VLAN for BPDU</b> 0 <sub>B</sub> Follows VLAN 1 <sub>B</sub> Crosses VLAN
NRTG	3:2	rw	<b>New Reserve TXTAG for GXP</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
NRTS	1:0	rw	<b>New Reserve TXTAG for SLOW/PAE/RESER_R0/RESER_R1/RESER_R2/RESER_R3</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged

Hardware IGMP Control Register

HIC Hardware IGMP Control Register Offset 3F<sub>H</sub> Reset Value 7C80<sub>H</sub>





Registers Description

Field	Bits	Type	Description
M	5:0	rw	<b>Member</b> These bits indicate which ports are the members of the VLAN.Member[x] Description. 0 <sub>B</sub> Port x is not a VLAN member 1 <sub>B</sub> Port x is a VLAN member

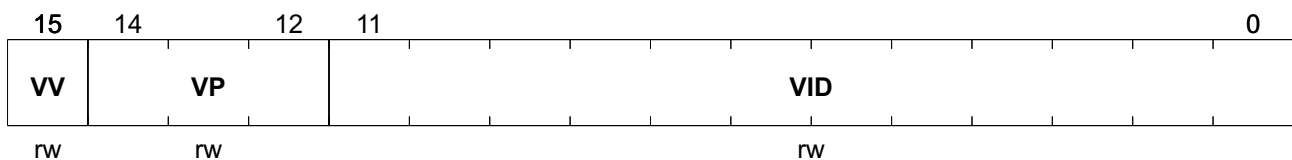
Similar Registers

Table 58 VFxL Registers

Register Short Name	Register Long Name	Offset Address	Page Number
VF1L	VLAN Filter 1 Low	42 <sub>H</sub>	
VF2L	VLAN Filter 2 Low	44 <sub>H</sub>	
VF3L	VLAN Filter 3Low	46 <sub>H</sub>	
VF4L	VLAN Filter 4 Low	48 <sub>H</sub>	
VF5L	VLAN Filter 5 Low	4A <sub>H</sub>	
VF6L	VLAN Filter 6 Low	4C <sub>H</sub>	
VF7L	VLAN Filter 7 Low	4E <sub>H</sub>	
VF8L	VLAN Filter 8 Low	50 <sub>H</sub>	
VF9L	VLAN Filter 9 Low	52 <sub>H</sub>	
VF10L	VLAN Filter 10 Low	54 <sub>H</sub>	
VF11L	VLAN Filter 11 Low	56 <sub>H</sub>	
VF12L	VLAN Filter 12 Low	58 <sub>H</sub>	
VF13L	VLAN Filter 13 Low	5A <sub>H</sub>	
VF14L	VLAN Filter 14 Low	5C <sub>H</sub>	
VF15L	VLAN Filter 15 Low	5E <sub>H</sub>	

VLAN Filter 0 High

<b>VF0H</b>	<b>Offset</b>	<b>Reset Value</b>
<b>VLAN Filter 0 High</b>	<b>41<sub>H</sub></b>	<b>8001<sub>H</sub></b>



Field	Bits	Type	Description
VV	15	rw	<b>VLAN_Valid</b> 0 <sub>B</sub> VLAN filter is not valid 1 <sub>B</sub> VLAN Filter is valid

Registers Description

Field	Bits	Type	Description
VP	14:12	rw	<b>VLAN PRI</b> It indicates the VLAN priority that is associated with VID.
VID	11:0	rw	<b>VID</b> It indicates the VLAN ID that is associated with FID, Tagged Member, Member and VLAN PRI.

**Similar Registers**

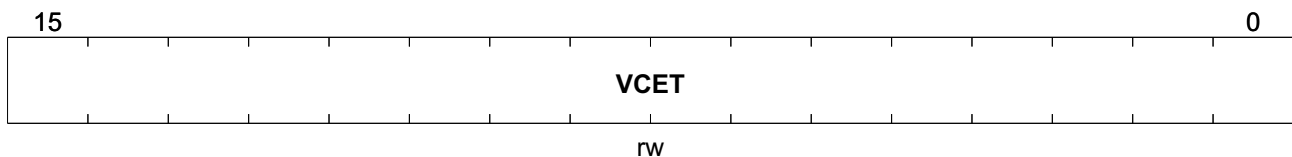
All VFxH registers have the same structure and characteristics, see [VF0H](#).  
The offset addresses of the other VFxH registers are listed in [Table 59](#).

**Table 59 VFxH Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
VF1H	VLAN Filter 1 High	43 <sub>H</sub>	
VF2H	VLAN Filter 2 High	45 <sub>H</sub>	
VF3H	VLAN Filter 3 High	47 <sub>H</sub>	
VF4H	VLAN Filter 4 High	49 <sub>H</sub>	
VF5H	VLAN Filter 5 High	4B <sub>H</sub>	
VF6H	VLAN Filter 6 High	4D <sub>H</sub>	
VF7H	VLAN Filter 7 High	4F <sub>H</sub>	
VF8H	VLAN Filter 8 High	51 <sub>H</sub>	
VF9H	VLAN Filter 9 High	53 <sub>H</sub>	
VF10H	VLAN Filter 10 High	55 <sub>H</sub>	
VF11H	VLAN Filter 11 High	57 <sub>H</sub>	
VF12H	VLAN Filter 12 High	59 <sub>H</sub>	
VF13H	VLAN Filter 13 High	5B <sub>H</sub>	
VF14H	VLAN Filter 14 High	5D <sub>H</sub>	
VF15H	VLAN Filter 15 High	5F <sub>H</sub>	

**Type Filter 0**

<b>TF0</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Type Filter 0</b>	<b>60<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
VCET	15:0	rw	<b>Value Compared with Ether-Type</b>

**Similar Registers**

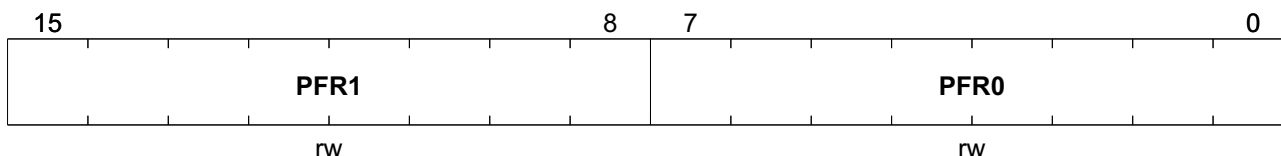
All TFx registers have the same structure and characteristics, see [TF0](#).  
The offset addresses of the other TFx registers are listed in [Table 60](#).

**Table 60** TFx Registers

Register Short Name	Register Long Name	Offset Address	Page Number
TF1	Type Filter 1	61 <sub>H</sub>	
TF2	Type Filter 2	62 <sub>H</sub>	
TF3	Type Filter 3	63 <sub>H</sub>	
TF4	Type Filter 4	64 <sub>H</sub>	
TF5	Type Filter 5	65 <sub>H</sub>	
TF6	Type Filter 6	66 <sub>H</sub>	
TF7	Type Filter 7	67 <sub>H</sub>	

**Protocol Filter 1 and 0**

**PF\_1\_0** **Offset**  
**Protocol Filter 1 and 0** **68<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
PFR1	15:8	rw	<b>Value Compared with Protocol in IP Header</b> (Protocol Filter 1, 3, 5, 7)
PFR0	7:0	rw	<b>Value Compared with Protocol in IP Header</b> (Protocol Filter 0, 2, 4, 6)

**Similar Registers**

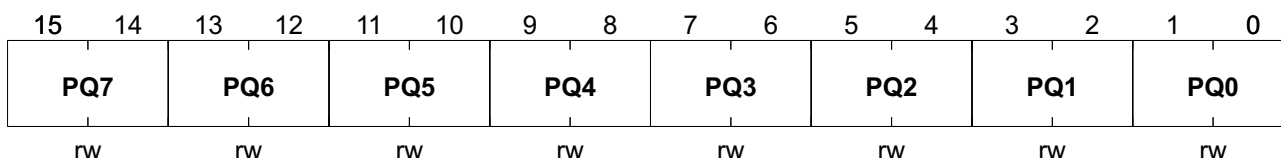
All PFx registers have the same structure and characteristics, see [PF\\_1\\_0](#).  
 The offset addresses of the other PFx registers are listed in [Table 61](#).

**Table 61 PFx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
PF_3_2	Protocol Filter 3 and 2	68 <sub>H</sub>	
PF_5_4	Protocol Filter 5 and 4	69 <sub>H</sub>	
PF_7_6	Protocol Filter 7 and 6	6A <sub>H</sub>	

**Service Priority Mapping 0**

**SPM0** **Offset**  
**Service Priority Mapping 0** **6C<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



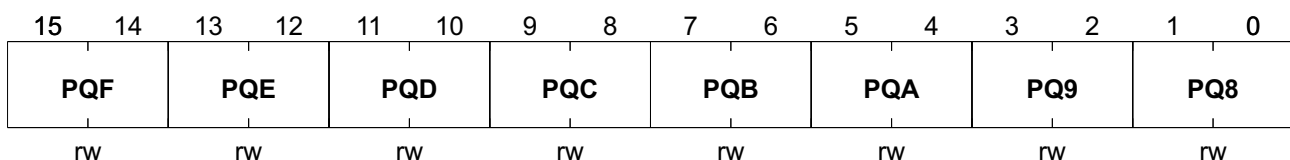
Field	Bits	Type	Description
PQ7	15:14	rw	<b>Priority Queue 7</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000111 <sub>B</sub> .

Registers Description

Field	Bits	Type	Description
PQ6	13:12	rw	<b>Priority Queue 6</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000110 <sub>B</sub> .
PQ5	11:10	rw	<b>Priority Queue 5</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000101 <sub>B</sub> .
PQ4	9:8	rw	<b>Priority Queue 4</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000100 <sub>B</sub> .
PQ3	7:6	rw	<b>Priority Queue 3</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000011 <sub>B</sub> .
PQ2	5:4	rw	<b>Priority Queue 2</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000010 <sub>B</sub> .
PQ1	3:2	rw	<b>Priority Queue 1</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000001 <sub>B</sub> .
PQ0	1:0	rw	<b>Priority Queue 0</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 000000 <sub>B</sub> . 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3

Service Priority Mapping 1

**SPM1** **Offset** **Reset Value**  
**Service Priority Mapping 1** **6D<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
PQF	15:14	rw	<b>Priority Queue F</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001111 <sub>B</sub> .
PQE	13:12	rw	<b>Priority Queue E</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001110 <sub>B</sub> .

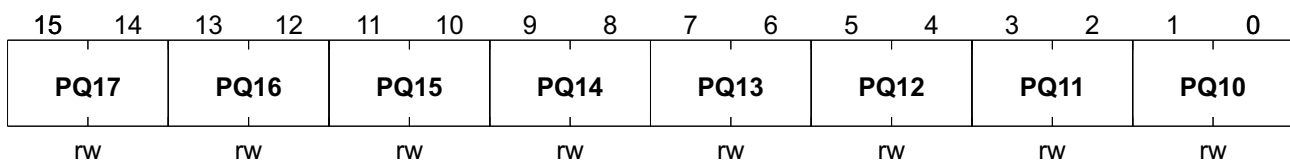


Registers Description

Field	Bits	Type	Description
PQD	11:10	rw	<b>Priority Queue D</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001101 <sub>B</sub>
PQC	9:8	rw	<b>Priority Queue C</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001100 <sub>B</sub>
PQB	7:6	rw	<b>Priority Queue B</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001011 <sub>B</sub>
PQA	5:4	rw	<b>Priority Queue A</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001010 <sub>B</sub>
PQ9	3:2	rw	<b>Priority Queue 9</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001001 <sub>B</sub>
PQ8	1:0	rw	<b>Priority Queue 8</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 001000 <sub>B</sub>

Service Priority Mapping 2

**SPM2** **Offset** **Reset Value**  
**Service Priority Mapping 2** **6E<sub>H</sub>** **0000<sub>H</sub>**



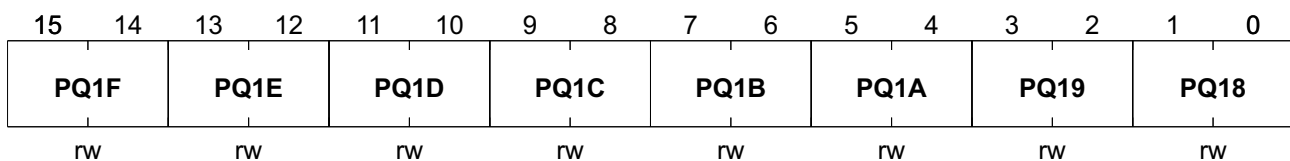
Field	Bits	Type	Description
PQ17	15:14	rw	<b>Priority Queue 17</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010111 <sub>B</sub>
PQ16	13:12	rw	<b>Priority Queue 16</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010110 <sub>B</sub>
PQ15	11:10	rw	<b>Priority Queue 15</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010101 <sub>B</sub>
PQ14	9:8	rw	<b>Priority Queue 14</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010100 <sub>B</sub>

Registers Description

Field	Bits	Type	Description
PQ13	7:6	rw	<b>Priority Queue 13</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010011 <sub>B</sub>
PQ12	5:4	rw	<b>Priority Queue 12</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010010 <sub>B</sub>
PQ11	3:2	rw	<b>Priority Queue 11</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010001 <sub>B</sub>
PQ10	1:0	rw	<b>Priority Queue 10</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 010000 <sub>B</sub>

Service Priority Mapping 3

SPM3 Offset Reset Value  
Service Priority Mapping 3 6F<sub>H</sub> 0000<sub>H</sub>



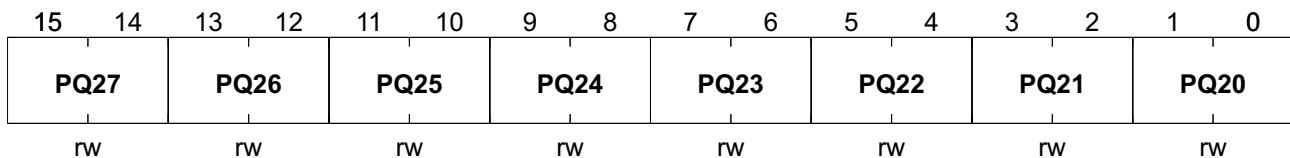
Field	Bits	Type	Description
PQ1F	15:14	rw	<b>Priority Queue 1F</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011111 <sub>B</sub>
PQ1E	13:12	rw	<b>Priority Queue 1E</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011110 <sub>B</sub>
PQ1D	11:10	rw	<b>Priority Queue 1D</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011101 <sub>B</sub>
PQ1C	9:8	rw	<b>Priority Queue 1C</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011100 <sub>B</sub>
PQ1B	7:6	rw	<b>Priority Queue 1B</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011011 <sub>B</sub>
PQ1A	5:4	rw	<b>Priority Queue 1A</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011010 <sub>B</sub>

Registers Description

Field	Bits	Type	Description
PQ19	3:2	rw	<b>Priority Queue 19</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011001 <sub>B</sub>
PQ18	1:0	rw	<b>Priority Queue 18</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 011000 <sub>B</sub>

Service Priority Mapping 4

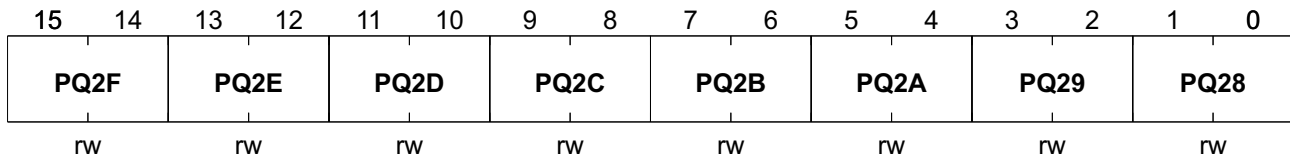
**SPM4** **Offset** **Reset Value**  
**Service Priority Mapping 4** **70<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
PQ27	15:14	rw	<b>Priority Queue 27</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100111 <sub>B</sub>
PQ26	13:12	rw	<b>Priority Queue 26</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100110 <sub>B</sub>
PQ25	11:10	rw	<b>Priority Queue 25</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100101 <sub>B</sub>
PQ24	9:8	rw	<b>Priority Queue 24</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100100 <sub>B</sub>
PQ23	7:6	rw	<b>Priority Queue 23</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100011 <sub>B</sub>
PQ22	5:4	rw	<b>Priority Queue 22</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100010 <sub>B</sub>
PQ21	3:2	rw	<b>Priority Queue 21</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100001 <sub>B</sub>
PQ20	1:0	rw	<b>Priority Queue 20</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 100000 <sub>B</sub>

Service Priority Mapping 5

**SPM5** **Offset** **Reset Value**  
**Service Priority Mapping 5** **71<sub>H</sub>** **0000<sub>H</sub>**

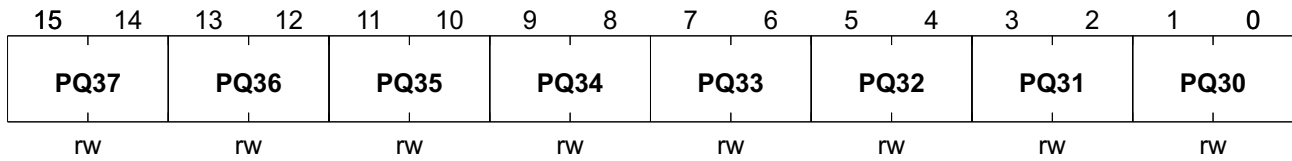


Field	Bits	Type	Description
PQ2F	15:14	rw	<b>Priority Queue 2F</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101111 <sub>B</sub>
PQ2E	13:12	rw	<b>Priority Queue 2E</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101110 <sub>B</sub>
PQ2D	11:10	rw	<b>Priority Queue 2D</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101101 <sub>B</sub>
PQ2C	9:8	rw	<b>Priority Queue 2C</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101100 <sub>B</sub>
PQ2B	7:6	rw	<b>Priority Queue 2B</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101011 <sub>B</sub>
PQ2A	5:4	rw	<b>Priority Queue 2A</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101010 <sub>B</sub>
PQ29	3:2	rw	<b>Priority Queue 29</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101001 <sub>B</sub>
PQ28	1:0	rw	<b>Priority Queue 28</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 101000 <sub>B</sub>

Service Priority Mapping 6

**SPM6** **Offset** **Reset Value**  
**Service Priority Mapping 6** **72<sub>H</sub>** **0000<sub>H</sub>**

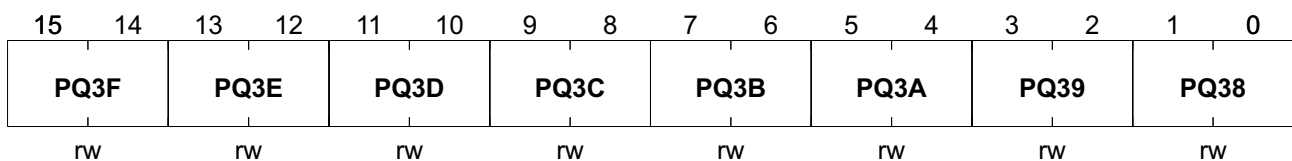
Registers Description



Field	Bits	Type	Description
PQ37	15:14	rw	<b>Priority Queue 37</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110111 <sub>B</sub>
PQ36	13:12	rw	<b>Priority Queue 36</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110110 <sub>B</sub>
PQ35	11:10	rw	<b>Priority Queue 35</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110101 <sub>B</sub>
PQ34	9:8	rw	<b>Priority Queue 34</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110100 <sub>B</sub>
PQ33	7:6	rw	<b>Priority Queue 33</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110011 <sub>B</sub>
PQ32	5:4	rw	<b>Priority Queue 32</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110010 <sub>B</sub>
PQ31	3:2	rw	<b>Priority Queue 31</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110001 <sub>B</sub>
PQ30	1:0	rw	<b>Priority Queue 30</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 110000 <sub>B</sub>

Service Priority Mapping 7

**SPM7** **Offset**  
**Service Priority Mapping 7** **73<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Registers Description

Field	Bits	Type	Description
PQ3F	15:14	rw	<b>Priority Queue 3F</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111111 <sub>B</sub>
PQ3E	13:12	rw	<b>Priority Queue 3E</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111110 <sub>B</sub>
PQ3D	11:10	rw	<b>Priority Queue 3D</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111101 <sub>B</sub>
PQ3C	9:8	rw	<b>Priority Queue 3C</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111100 <sub>B</sub>
PQ3B	7:6	rw	<b>Priority Queue 3B</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111011 <sub>B</sub>
PQ3A	5:4	rw	<b>Priority Queue 3A</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111010 <sub>B</sub>
PQ39	3:2	rw	<b>Priority Queue 39</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111001 <sub>B</sub>
PQ38	1:0	rw	<b>Priority Queue 38</b> The value in this field is used as the priority queue when the significant 6 bits in the IPV4 TOS/IPV6 Traffic Class are 111000 <sub>B</sub>

Reserve Action for 0180C2000001~0180C2000000

<b>RA_01_00</b>	<b>Offset</b>	<b>Reset Value</b>
Reserve Action for 0180C2000001~0180C2000000	74 <sub>H</sub>	0000 <sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RA01 _VA*	RA01 _SP*	RA01 _MG	RA01 _CV	RA01_TX TAG	RA01_AC T	RA00 _VA*	RA00 _SP*	RA00 _MG	RA00 _CV	RA00_TX TAG	RA00_AC T				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw			

Field	Bits	Type	Description
RA01_VALID	15	rw	<b>Valid bit for 0180C2000001</b> 0 <sub>B</sub> Not Valid 1 <sub>B</sub> Valid

Registers Description

Field	Bits	Type	Description
RA01_SPAN	14	rw	<b>Span bit for 0180C2000001</b> 0 <sub>B</sub> Doesn't identify as the span packet 1 <sub>B</sub> Identifies as the span packet
RA01_MG	13	rw	<b>Management bit for 0180C2000001</b> 0 <sub>B</sub> Doesn't identify as the management packet 1 <sub>B</sub> Identifies as the management packet
RA01_CV	12	rw	<b>Cross_VLAN bit for 0180C2000001</b> 0 <sub>B</sub> Doesn't identify as the cross_VLAN packet 1 <sub>B</sub> Identifies as the cross_VLAN packet
RA01_TXTAG	11:10	rw	<b>TXTAG bit for 0180C2000001</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
RA01_ACT	9:8	rw	<b>Action bit for 0180C2000001</b> 00 <sub>B</sub> Portmap is 111111 <sub>B</sub> 01 <sub>B</sub> Portmap is 000000 <sub>B</sub> 10 <sub>B</sub> Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port 11 <sub>B</sub> Portmap contains all the ports, excluding the CPU port
RA00_VALID	7	rw	<b>Valid bit for 0180C2000000</b> 0 <sub>B</sub> Not Valid 1 <sub>B</sub> Valid
RA00_SPAN	6	rw	<b>Span bit for 0180C2000000</b> 0 <sub>B</sub> Doesn't identify as the span packet 1 <sub>B</sub> Identifies as the span packet
RA00_MG	5	rw	<b>Management bit for 0180C2000000</b> 0 <sub>B</sub> Doesn't identify as the management packet 1 <sub>B</sub> Identifies as the management packet
RA00_CV	4	rw	<b>Cross_VLAN bit for 0180C2000000</b> 0 <sub>B</sub> Doesn't identify as the cross_VLAN packet 1 <sub>B</sub> Identifies as the cross_VLAN packet
RA00_TXTAG	3:2	rw	<b>TXTAG bit for 0180C2000000</b> 00 <sub>B</sub> System Default Tag 01 <sub>B</sub> Unmodified 10 <sub>B</sub> Always Tagged 11 <sub>B</sub> Always Untagged
RA00_ACT	1:0	rw	<b>Action bit for 0180C2000000</b> 00 <sub>B</sub> Portmap is 111111 <sub>B</sub> 01 <sub>B</sub> Portmap is 000000 <sub>B</sub> 10 <sub>B</sub> Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Reserve Portmap contains all the ports, excluding the CPU port 11 <sub>B</sub> Portmap contains all the ports, excluding the CPU port

**Similar Registers**

All RAx registers have the same structure and characteristics, see [RA\\_01\\_00](#).  
The offset addresses of the other RAx registers are listed in [Table 62](#).

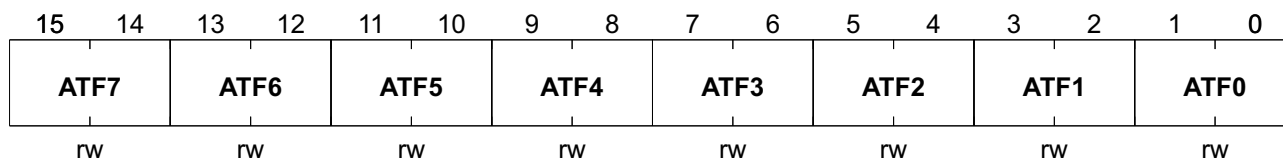
**Table 62 RAx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
RA_03_02	Reserve Action for 0180C2000003~0180C2000002	75 <sub>H</sub>	
RA_05_04	Reserve Action for 0180C2000005~0180C2000004	76 <sub>H</sub>	
RA_07_06	Reserve Action for 0180C2000007~0180C2000006	77 <sub>H</sub>	
RA_09_08	Reserve Action for 0180C2000009~0180C2000008	78 <sub>H</sub>	
RA_0B_0A	Reserve Action for 0180C200000B~0180C200000A	79 <sub>H</sub>	
RA_0D_0C	Reserve Action for 0180C200000D~0180C200000C	7A <sub>H</sub>	
RA_0F_0E	Reserve Action for 0180C200000F~0180C200000E	7B <sub>H</sub>	
RA_11_10	Reserve Action for 0180C2000011~0180C2000010	7C <sub>H</sub>	
RA_13_12	Reserve Action for 0180C2000013~0180C2000012	7D <sub>H</sub>	
RA_15_14	Reserve Action for 0180C2000015~0180C2000014	7E <sub>H</sub>	
RA_17_16	Reserve Action for 0180C2000017~0180C2000016	7F <sub>H</sub>	
RA_19_18	Reserve Action for 0180C2000019~0180C2000018	80 <sub>H</sub>	
RA_1B_1A	Reserve Action for 0180C200001B~0180C200001A	81 <sub>H</sub>	
RA_1D_1C	Reserve Action for 0180C200001D~0180C200001C	82 <sub>H</sub>	
RA_1F_1E	Reserve Action for 0180C200001F~0180C200001E	83 <sub>H</sub>	
RA_21_20	Reserve Action for 0180C2000021~0180C2000020	84 <sub>H</sub>	
RA_23_22	Reserve Action for 0180C2000023~0180C2000022	85 <sub>H</sub>	
RA_25_24	Reserve Action for 0180C2000025~0180C2000024	86 <sub>H</sub>	
RA_27_26	Reserve Action for 0180C2000027~0180C2000026	87 <sub>H</sub>	
RA_29_28	Reserve Action for 0180C2000029~0180C2000028	88 <sub>H</sub>	





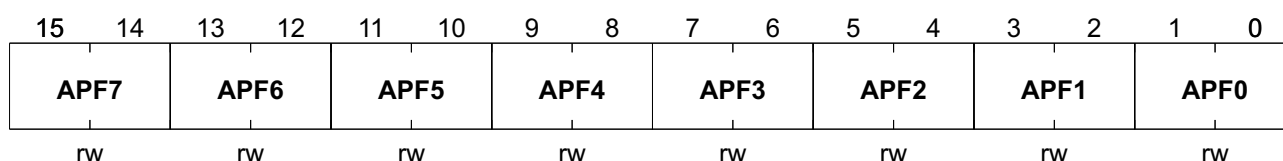
Registers Description



Field	Bits	Type	Description
ATF7	15:14	rw	<b>Action for Type Filter 7</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF6	13:12	rw	<b>Action for Type Filter 6</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF5	11:10	rw	<b>Action for Type Filter 5</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF4	9:8	rw	<b>Action for Type Filter 4</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF3	7:6	rw	<b>Action for Type Filter 3</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF2	5:4	rw	<b>Action for Type Filter 2</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF1	3:2	rw	<b>Action for Type Filter 1</b> See register 0094 <sub>H</sub> , <a href="#">ATF0</a> for more details.
ATF0	1:0	rw	<b>Action for Type Filter 0</b> 00 <sub>B</sub> Type Portmap is Default Output Ports 01 <sub>B</sub> Type Portmap is 000000 <sub>B</sub> 10 <sub>B</sub> Type Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports , excluding the CPU port 11 <sub>B</sub> Type Portmap contains Default Output Port, excluding the CPU port

Protocol Filter Action

<b>PFA</b>	<b>Offset</b>	<b>Reset Value</b>
Protocol Filter Action	95 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
APF7	15:14	rw	<b>Action for Protocol Filter 7</b> See register 0095 <sub>H</sub> , <a href="#">APF0</a> for more details.

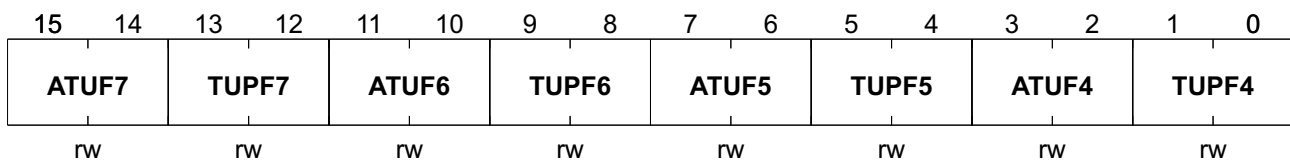


Registers Description

Field	Bits	Type	Description
TUPF1	5:4	rw	<b>TCP/UDP PRI for TCP/UDP Filter 1</b> See register 0096 <sub>H</sub> , <a href="#">TUPF0</a> for more details.
ATUF0	3:2	rw	<b>Action for TCP/UDP Filter 0</b> 00 <sub>B</sub> Protocol Portmap is Default Output Ports 01 <sub>B</sub> Protocol Portmap is 000000 <sub>B</sub> 10 <sub>B</sub> Protocol Portmap is the CPU port if the incoming port is not the CPU port. But if the incoming port is the CPU port, then Type Portmap contains Default Output Ports, excluding the CPU port 11 <sub>B</sub> Protocol Portmap contains Default Output Ports, excluding the CPU port
TUPF0	1:0	rw	<b>TCP/UDP PRI for TCP/UDP Filter 0</b> 00 <sub>B</sub> Queue 0 01 <sub>B</sub> Queue 1 10 <sub>B</sub> Queue 2 11 <sub>B</sub> Queue 3

TCP/UDP Action 1

TUA1	Offset	Reset Value
TCP/UDP Action 1	97 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
ATUF7	15:14	rw	<b>Action for TCP/UDP Filter 7</b> See register 0096 <sub>H</sub> , <a href="#">ATUF0</a> for more details.
TUPF7	13:12	rw	<b>TCP/UDP PRI for TCP/UDP Filter 7</b> See register 0096 <sub>H</sub> , <a href="#">TUPF0</a> for more details.
ATUF6	11:10	rw	<b>Action for TCP/UDP Filter 6</b> See register 0096 <sub>H</sub> , <a href="#">ATUF0</a> for more details.
TUPF6	9:8	rw	<b>TCP/UDP PRI for TCP/UDP Filter 6</b> See register 0096 <sub>H</sub> , <a href="#">TUPF0</a> for more details.
ATUF5	7:6	rw	<b>Action for TCP/UDP Filter 5</b> See register 0096 <sub>H</sub> , <a href="#">ATUF0</a> for more details.
TUPF5	5:4	rw	<b>TCP/UDP PRI for TCP/UDP Filter 5</b> See register 0096 <sub>H</sub> , <a href="#">TUPF0</a> for more details.
ATUF4	3:2	rw	<b>Action for TCP/UDP Filter 4</b> See register 0096 <sub>H</sub> , <a href="#">ATUF0</a> for more details.
TUPF4	1:0	rw	<b>TCP/UDP PRI for TCP/UDP Filter 4</b> See register 0096 <sub>H</sub> , <a href="#">TUPF0</a> for more details.

TCP/UDP Action 2

TUA2  
TCP/UDP Action 2

Offset  
98<sub>H</sub>

Reset Value  
0000<sub>H</sub>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		COMP		P5I	P4I	P3I	P2I	P1I	P0I	P5T	P4T	P3T	P2T	P1T	P0T
r		rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:14	r	<b>Reserved</b>
COMP	13:12	rw	<b>Compare TCP/UDP Source Port or Destination Port</b> 00 <sub>B</sub> Doesn't Compare 01 <sub>B</sub> Compares Destination Port 10 <sub>B</sub> Compares Source Port 11 <sub>B</sub> Compares Destination Port or Source Port
P5I	11	rw	<b>Port 5 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P4I	10	rw	<b>Port 4 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P3I	9	rw	<b>Port 3 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P2I	8	rw	<b>Port 2 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P1I	7	rw	<b>Port 1 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P0I	6	rw	<b>Port 0 IP over TCP/UDP</b> 0 <sub>B</sub> Uses TCP/UDP field when packets contain both TCP/UDP and IP 1 <sub>B</sub> Uses IP field when packets contain both TCP/UDP and IP
P5T	5	rw	<b>Port 5 TCP/UDP PRIEN</b> 0 <sub>B</sub> Doesn't use TCP/UDP priority 1 <sub>B</sub> Uses TCP/UDP priority
P4T	4	rw	<b>Port 4 TCP/UDP PRIEN</b> 0 <sub>B</sub> Doesn't use TCP/UDP priority 1 <sub>B</sub> Uses TCP/UDP priority
P3T	3	rw	<b>Port 3 TCP/UDP PRIEN</b> 0 <sub>B</sub> Doesn't use TCP/UDP priority 1 <sub>B</sub> Uses TCP/UDP priority

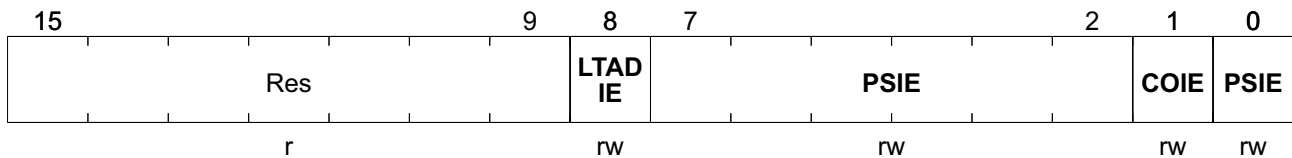


Registers Description

Field	Bits	Type	Description
INS_PROT	3	rw	<b>Insert Special Tag if Protocol field matches with pre-defined rules.</b> 0 <sub>B</sub> Doesn't insert 1 <sub>B</sub> Inserts
INS_TU	2	rw	<b>Insert Special Tag if Port field matches with pre-defined rules.</b> 0 <sub>B</sub> Doesn't insert 1 <sub>B</sub> Inserts
INS_MC	1	rw	<b>Insert Special Tag in MAC Control Packet.</b> 0 <sub>B</sub> Doesn't insert 1 <sub>B</sub> Inserts
INS_DEF	0	rw	<b>Insert Special Tag in the packets except those packets defined in bit 8 ~ 1.</b> 0 <sub>B</sub> Doesn't insert 1 <sub>B</sub> Inserts

Interrupt Enable Register

**IE** **Offset**  
**Interrupt Enable Register** **9A<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
Res	15:9	r	<b>Reserved</b>
LTADIE	8	rw	<b>Leaning Table Access Done Interrupt Enable</b> 0 <sub>B</sub> Interrupt disable 1 <sub>B</sub> Interrupt enable
PSIE	7:2	rw	<b>Port Security Interrupt Enable</b> It's a per port setting 0 <sub>B</sub> Interrupt disable 1 <sub>B</sub> Interrupt enable
COIE	1	rw	<b>Counter Overflow Interrupt Enable</b> 0 <sub>B</sub> Interrupt disable 1 <sub>B</sub> Interrupt enable
PSIE	0	rw	<b>Port Status Interrupt Enable</b> 0 <sub>B</sub> Interrupt disable 1 <sub>B</sub> Interrupt enable

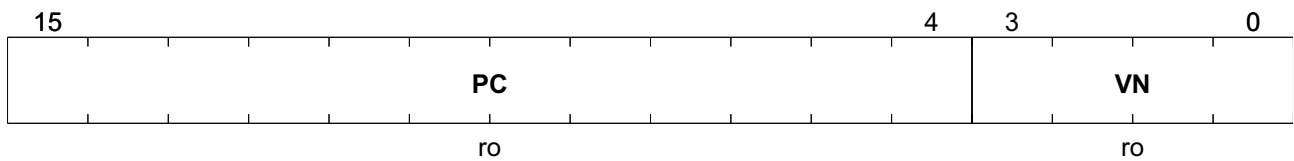




### 4.3 Counter and Switch Status Registers

#### Chip Identifier 0

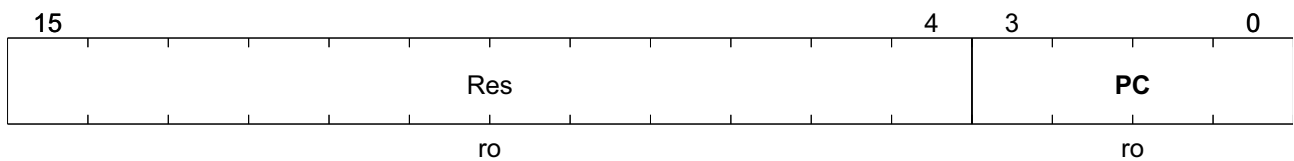
**C10** Offset **Reset Value**  
Chip Identifier 0 **A0<sub>H</sub>** **1023<sub>H</sub>**



Field	Bits	Type	Description
PC	15:4	ro	Product Code[11:0]
VN	3:0	ro	Version Number

#### Chip Identifier 1

**C11** Offset **Reset Value**  
Chip Identifier 1 **A1<sub>H</sub>** **0007<sub>H</sub>**

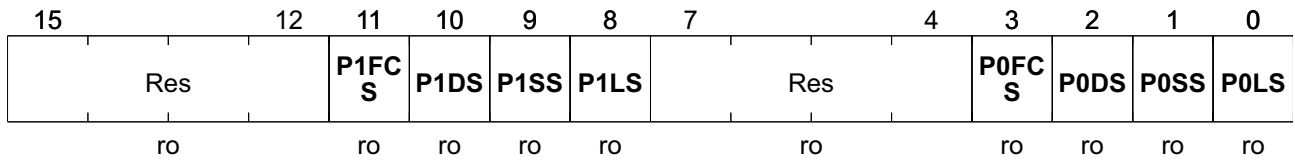


Field	Bits	Type	Description
Res	15:4	ro	Reserved
PC	3:0	ro	Product Code[ 15:12 ]

#### Port Status 0

**PS0** Offset **Reset Value**  
Port Status 0 **A2<sub>H</sub>** **0000<sub>H</sub>**

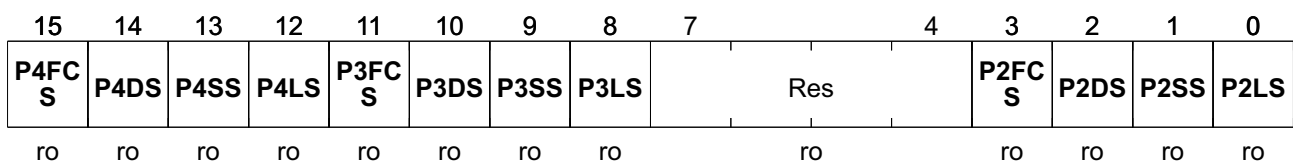
Registers Description



Field	Bits	Type	Description
Res	15:12	ro	<b>Reserved</b>
P1FCS	11	ro	<b>Port 1 Flow Control Status</b> 0 <sub>B</sub> Port 1 disables the Full Flow Control/Half Back Pressure Function 1 <sub>B</sub> Port 1 enables the Full Flow Control/Half Back Pressure Function
P1DS	10	ro	<b>Port 1 Duplex Status</b> 0 <sub>B</sub> Port 1 operates in the Half Duplex 1 <sub>B</sub> Port 1 operates in the Full Duplex
P1SS	9	ro	<b>Port 1 Speed Status</b> 0 <sub>B</sub> Port 1 operates in the 10M 1 <sub>B</sub> Port 1 operates in the 100M
P1LS	8	ro	<b>Port 1 Link Status</b> 0 <sub>B</sub> Port 1 links down 1 <sub>B</sub> Port 1 links up
Res	7:4	ro	<b>Reserved</b>
P0FCS	3	ro	<b>Port 0 Flow Control Status</b> 0 <sub>B</sub> Port 0 disables the Full Flow Control/Half Back Pressure Function 1 <sub>B</sub> Port 0 enables the Full Flow Control/Half Back Pressure Function
P0DS	2	ro	<b>Port 0 Duplex Status</b> 0 <sub>B</sub> Port 0 operates in the Half Duplex 1 <sub>B</sub> Port 0 operates in the Full Duplex
P0SS	1	ro	<b>Port 0 Speed Status</b> 0 <sub>B</sub> Port 0 operates in the 10M 1 <sub>B</sub> Port 0 operates in the 100M
P0LS	0	ro	<b>Port 0 Link Status</b> 0 <sub>B</sub> Port 0 links down 1 <sub>B</sub> Port 0 links up

**Port Status 1**

<b>PS1</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Port Status 1</b>	<b>A3<sub>H</sub></b>	<b>0000<sub>H</sub></b>

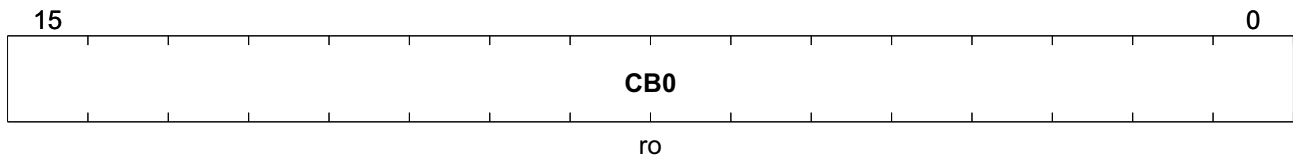


Field	Bits	Type	Description
P4FCS	15	ro	<b>Port 4 Flow Control Status</b> 0 <sub>B</sub> Port 4 disables the Full Flow Control/Half Back Pressure Function 1 <sub>B</sub> Port 4 enables the Full Flow Control/Half Back Pressure Function
P4DS	14	ro	<b>Port 4 Duplex Status</b> 0 <sub>B</sub> Port 4 operates in the Half Duplex 1 <sub>B</sub> Port 4 operates in the Full Duplex
P4SS	13	ro	<b>Port 4 Speed Status</b> 0 <sub>B</sub> Port 4 operates in the 10M 1 <sub>B</sub> Port 4 operates in the 100M
P4LS	12	ro	<b>Port 4 Link Status</b> 0 <sub>B</sub> Port 4 links down 1 <sub>B</sub> Port 4 links up
P3FCS	11	ro	<b>Port 3 Flow Control Status</b> 0 <sub>B</sub> Port 3 disables the Full Flow Control/Half Back Pressure Function 1 <sub>B</sub> Port 3 enables the Full Flow Control/Half Back Pressure Function
P3DS	10	ro	<b>Port 3 Duplex Status</b> 0 <sub>B</sub> Port 3 operates in the Half Duplex 1 <sub>B</sub> Port 3 operates in the Full Duplex
P3SS	9	ro	<b>Port 3 Speed Status</b> 0 <sub>B</sub> Port 3 operates in the 10M 1 <sub>B</sub> Port 3 operates in the 100M
P3LS	8	ro	<b>Port 3 Link Status</b> 0 <sub>B</sub> Port 3 links down 1 <sub>B</sub> Port 3 links up.
Res	7:4	ro	<b>Reserved</b>
P2FCS	3	ro	<b>Port 2 Flow Control Status</b> 0 <sub>B</sub> Port 2 disables the Full Flow Control/Half Back Pressure Function 1 <sub>B</sub> Port 2 enables the Full Flow Control/Half Back Pressure Function
P2DS	2	ro	<b>Port 2 Duplex Status</b> 0 <sub>B</sub> Port 2 operates in the Half Duplex 1 <sub>B</sub> Port 2 operates in the Full Duplex
P2SS	1	ro	<b>Port 2 Speed Status</b> 0 <sub>B</sub> Port 2 operates in the 10M 1 <sub>B</sub> Port 2 operates in the 100M
P2LS	0	ro	<b>Port 2 Link Status</b> 0 <sub>B</sub> Port 2 links down 1 <sub>B</sub> Port 2 links up

**Port Status 2**

PS2	Offset	Reset Value
Port Status 2	A4 <sub>H</sub>	0000 <sub>H</sub>

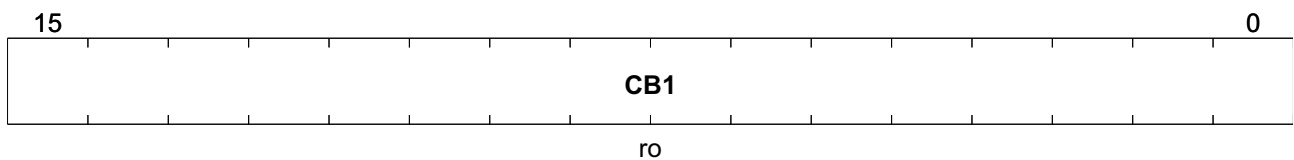




Field	Bits	Type	Description
CB0	15:0	ro	Reserved

### Cable Broken 1

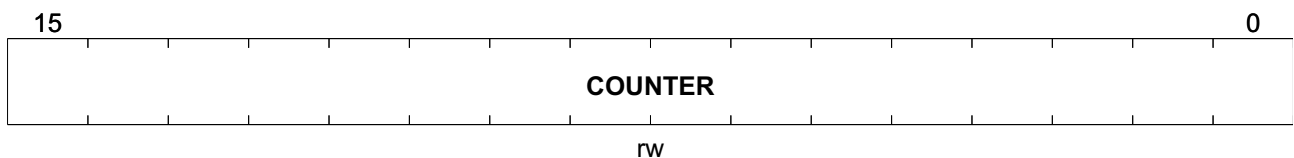
CB1	Offset	Reset Value
Cable Broken 1	A7 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
CB1	15:0	ro	Reserved

### Counter Low 0

CL0	Offset	Reset Value
Port 0 Receive Packet Counter Low	A8 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
COUNTER	15:0	rw	Counter[15:0]

### Similar Registers

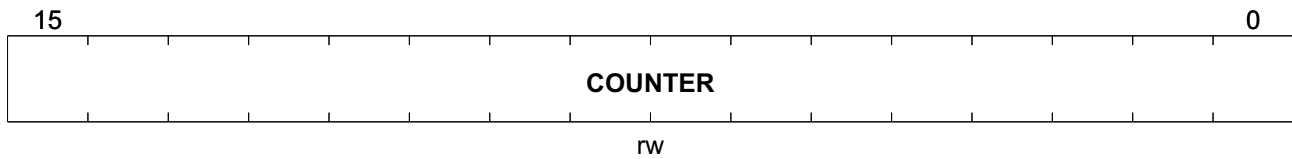
All CLx registers have the same structure and characteristics, see [CL0](#).  
The offset addresses of the other CLx registers are listed in [Table 64](#).

**Table 64 CLx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
CL1	Port 1 Receive Packet Counter Low	AC <sub>H</sub>	
CL2	Port 2 Receive Packet Counter Low	B0 <sub>H</sub>	
CL3	Port 3 Receive Packet Counter Low	B4 <sub>H</sub>	
CL4	Port 4 Receive Packet Counter Low	B6 <sub>H</sub>	
CL5	Port 5 Receive Packet Counter Low	B8 <sub>H</sub>	
CL6	Port 0 Receive Packet Byte Count Low	BA <sub>H</sub>	
CL7	Port 1 Receive Packet Byte Count Low	BE <sub>H</sub>	
CL8	Port 2 Receive Packet Byte Count Low	C2 <sub>H</sub>	
CL9	Port 3 Receive Packet Byte Count Low	C6 <sub>H</sub>	
CL10	Port 4 Receive Packet Byte Count Low	C8 <sub>H</sub>	
CL11	Port 5 Receive Packet Byte Count Low	CA <sub>H</sub>	
CL12	Port 0 Transmit Packet Count Low	CC <sub>H</sub>	
CL13	Port 1 Transmit Packet Count Low	D0 <sub>H</sub>	
CL14	Port 2 Transmit Packet Count Low	D4 <sub>H</sub>	
CL15	Port 3 Transmit Packet Count Low	D8 <sub>H</sub>	
CL16	Port 4 Transmit Packet Count Low	DA <sub>H</sub>	
CL17	Port 5 Transmit Packet Count Low	DC <sub>H</sub>	
CL18	Port 0 Transmit Packet Byte Count Low	DE <sub>H</sub>	
CL19	Port 1 Transmit Packet Byte Count Low	E2 <sub>H</sub>	
CL20	Port 2 Transmit Packet Byte Count Low	E6 <sub>H</sub>	
CL21	Port 3 Transmit Packet Byte Count Low	EA <sub>H</sub>	
CL22	Port 4 Transmit Packet Byte Count Low	EC <sub>H</sub>	
CL23	Port 5 Transmit Packet Byte Count Low	EE <sub>H</sub>	
CL24	Port 0 Collision Count Low	F0 <sub>H</sub>	
CL25	Port 1 Collision Count Low	F4 <sub>H</sub>	
CL26	Port 2 Collision Count Low	F8 <sub>H</sub>	
CL27	Port 3 Collision Count Low	FC <sub>H</sub>	
CL28	Port 4 Collision Count Low	FE <sub>H</sub>	
CL29	Port 5 Collision Count Low	100 <sub>H</sub>	
CL30	Port 0 Error Count Low	102 <sub>H</sub>	
CL31	Port 1 Error Count Low	106 <sub>H</sub>	
CL32	Port 2 Error Count Low	10A <sub>H</sub>	
CL33	Port 3 Error Count Low	10E <sub>H</sub>	
CL34	Port 4 Error Count Low	110 <sub>H</sub>	
CL35	Port 5 Error Count Low	112 <sub>H</sub>	

**Counter High 0**

<b>CH0</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Port 0 Receive Packet Counter High</b>	<b>A9<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
COUNTER	15:0	rw	Counter[31:16]

### Similar Registers

All CHx registers have the same structure and characteristics, see [CH0](#).  
The offset addresses of the other CLH registers are listed in [Table 65](#).

**Table 65 CHx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
CH1	Port 1 Receive Packet Counter High	AD <sub>H</sub>	
CH2	Port 2 Receive Packet Counter High	B1 <sub>H</sub>	
CH3	Port 3 Receive Packet Counter High	B5 <sub>H</sub>	
CH4	Port 4 Receive Packet Counter High	B7 <sub>H</sub>	
CH5	Port 5 Receive Packet Counter High	B9 <sub>H</sub>	
CH6	Port 0 Receive Packet Byte Count High	BB <sub>H</sub>	
CH7	Port 1 Receive Packet Byte Count High	BF <sub>H</sub>	
CH8	Port 2 Receive Packet Byte Count High	C3 <sub>H</sub>	
CH9	Port 3 Receive Packet Byte Count High	C7 <sub>H</sub>	
CH10	Port 4 Receive Packet Byte Count High	C9 <sub>H</sub>	
CH11	Port 5 Receive Packet Byte Count High	CB <sub>H</sub>	
CH12	Port 0 Transmit Packet Count High	CD <sub>H</sub>	
CH13	Port 1 Transmit Packet Count High	D1 <sub>H</sub>	
CH14	Port 2 Transmit Packet Count High	D5 <sub>H</sub>	
CH15	Port 3 Transmit Packet Count High	D9 <sub>H</sub>	
CH16	Port 4 Transmit Packet Count High	DB <sub>H</sub>	
CH17	Port 5 Transmit Packet Count High	DD <sub>H</sub>	
CH18	Port 0 Transmit Packet Byte Count High	DF <sub>H</sub>	
CH19	Port 1 Transmit Packet Byte Count High	E3 <sub>H</sub>	
CH20	Port 2 Transmit Packet Byte Count High	E7 <sub>H</sub>	
CH21	Port 3 Transmit Packet Byte Count High	EB <sub>H</sub>	
CH22	Port 4 Transmit Packet Byte Count High	ED <sub>H</sub>	
CH23	Port 5 Transmit Packet Byte Count High	EF <sub>H</sub>	
CH24	Port 0 Collision Count High	F1 <sub>H</sub>	
CH25	Port 1 Collision Count High	F5 <sub>H</sub>	
CH26	Port 2 Collision Count High	F9 <sub>H</sub>	
CH27	Port 3 Collision Count High	FD <sub>H</sub>	
CH28	Port 4 Collision Count High	FF <sub>H</sub>	

**Table 65 CHx Registers (cont'd)**

Register Short Name	Register Long Name	Offset Address	Page Number
CH29	Port 5 Collision Count High	101 <sub>H</sub>	
CH30	Port 0 Error Count High	103 <sub>H</sub>	
CH31	Port 1 Error Count High	107 <sub>H</sub>	
CH32	Port 2 Error Count High	10B <sub>H</sub>	
CH33	Port 3 Error Count High	10F <sub>H</sub>	
CH34	Port 4 Error Count High	111 <sub>H</sub>	
CH35	Port 5 Error Count High	113 <sub>H</sub>	

**Over-Flow Flag 0**

<b>OFF0</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Over-Flow Flag 0</b>	<b>114<sub>H</sub></b>	<b>0000<sub>H</sub></b>

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>P3_B C</b>	Res	<b>P2_B C</b>	Res	<b>P1_B C</b>	Res	<b>P0_B C</b>	<b>P5_C</b>	<b>P4_C</b>	<b>P3_C</b>	Res	<b>P2_C</b>	Res	<b>P1_C</b>	Res	<b>P0_C</b>
lhsc	ro	lhsc	ro	lhsc	ro	lhsc	lhsc	lhsc	lhsc	ro	lhsc	ro	lhsc	ro	lhsc

Field	Bits	Type	Description
P3_BC	15	lhsc	<b>Overflow of Port 3 Receive Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	14	ro	<b>Reserved</b>
P2_BC	13	lhsc	<b>Overflow of Port 2 Receive Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	12	ro	<b>Reserved</b>
P1_BC	11	lhsc	<b>Overflow of Port 1 Receive Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	10	ro	<b>Reserved</b>
P0_BC	9	lhsc	<b>Overflow of Port 0 Receive Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P5_C	8	lhsc	<b>Overflow of Port 5 Receive Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P4_C	7	lhsc	<b>Overflow of Port 4 Receive Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow





Registers Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P3_B C	Res	P2_B C	Res	P1_B C	Res	P0_B C	P5_C	P4_C	P3_C	Res	P2_C	Res	P1_C	Res	P0_C
lhsc	ro	lhsc	ro	lhsc	ro	lhsc	lhsc	lhsc	lhsc	ro	lhsc	ro	lhsc	ro	lhsc

Field	Bits	Type	Description
P3_BC	15	lhsc	<b>Overflow of Port 3 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	14	ro	<b>Reserved</b>
P2_BC	13	lhsc	<b>Overflow of Port 2 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	12	ro	<b>Reserved</b>
P1_BC	11	lhsc	<b>Overflow of Port 1 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	10	ro	<b>Reserved</b>
P0_BC	9	lhsc	<b>Overflow of Port 0 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P5_C	8	lhsc	<b>Overflow of Port 5 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P4_C	7	lhsc	<b>Overflow of Port 4 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P3_C	6	lhsc	<b>Overflow of Port 3 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	5	ro	<b>Reserved</b>
P2_C	4	lhsc	<b>Overflow of Port 2 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	3	ro	<b>Reserved</b>
P1_C	2	lhsc	<b>Overflow of Port 1 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	1	ro	<b>Reserved</b>
P0_C	0	lhsc	<b>Overflow of Port 0 Transmit Packet Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow

Over-Flow Flag 3

Registers Description

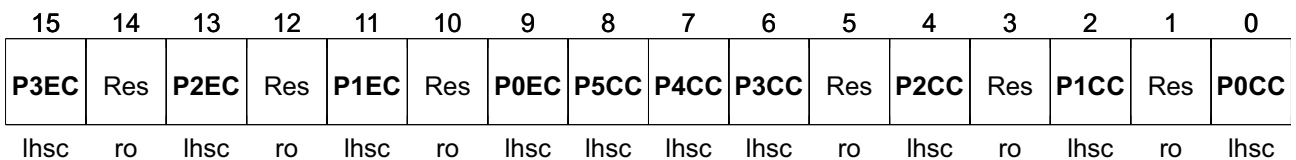
**OFF3** **Offset** **Reset Value**  
**Over-Flow Flag 3** **117<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
Res	15:2	ro	<b>Reserved</b>
P5_BC	1	lhsc	<b>Overflow of Port 5 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P4_BC	0	lhsc	<b>Overflow of Port 4 Transmit Packet Byte Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow

**Over-Flow Flag 4**

**OFF4** **Offset** **Reset Value**  
**Over-Flow Flag 4** **118<sub>H</sub>** **0000<sub>H</sub>**



Field	Bits	Type	Description
P3EC	15	lhsc	<b>Overflow of Port 3 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	14	ro	<b>Reserved</b>
P2EC	13	lhsc	<b>Overflow of Port 2 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	12	ro	<b>Reserved</b>
P1EC	11	lhsc	<b>Overflow of Port 1 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	10	ro	<b>Reserved</b>

Registers Description

Field	Bits	Type	Description
P0EC	9	lhsc	<b>Overflow of Port 0 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P5CC	8	lhsc	<b>Overflow of Port 5 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P4CC	7	lhsc	<b>Overflow of Port 4 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P3CC	6	lhsc	<b>Overflow of Port 3 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	5	ro	<b>Reserved</b>
P2CC	4	lhsc	<b>Overflow of Port 2 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	3	ro	<b>Reserved</b>
P1CC	2	lhsc	<b>Overflow of Port 1 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
Res	1	ro	<b>Reserved</b>
P0CC	0	lhsc	<b>Overflow of Port 0 Collision Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow

Over-Flow Flag 5

<b>OFF5</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Over-Flow Flag 5</b>	<b>119<sub>H</sub></b>	<b>0000<sub>H</sub></b>



Field	Bits	Type	Description
Res	15:2	ro	<b>Reserved</b>
P5EC	1	lhsc	<b>Overflow of Port 5 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow
P4EC	0	lhsc	<b>Overflow of Port 4 Error Count</b> 0 <sub>B</sub> No overflow 1 <sub>B</sub> Overflow

Hardware Setting Low Register

**HSL** Offset **Reset Value**  
**Hardware Setting Low Register** **130<sub>H</sub>** **0000<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H	BO	DAF	BP	DB	GM	RM	P4IT		GFC	P4FM	DC	CA		AC	AN
ro	ro	ro	ro	ro	ro	ro	ro		ro	ro	ro	ro		ro	ro

Field	Bits	Type	Description
H	15	ro	Reserved
BO	14	ro	Bond
DAF	13	ro	Disable Samurai-6M/6MX (ADM6996M/MX) Function
BP	12	ro	BPEN
DB	11	ro	16/32 Bit Data Bus
GM	10	ro	GPSI Mode
RM	9	ro	RMI Mode
P4IT	8:7	ro	Port 4 Interface Type
GFC	6	ro	Global Flow Control
P4FM	5	ro	Port 4 Fiber Mode
DC	4	ro	Dual Color
CA	3:2	ro	Chip Address
AC	1	ro	Auto-Crossover
AN	0	ro	Auto-Negotiation

Hardware Setting High Register

**HSH** Offset **Reset Value**  
**Hardware Setting High Register** **131<sub>H</sub>** **0000<sub>H</sub>**

15					10	9	8	7	6	5	4	3	2	1	0
Res					LTBR	LLTB R	CTBR	HITB R	DBBR	P5M		P4M		CFG	
ro					ro	ro	ro	ro	ro	ro		ro		ro	

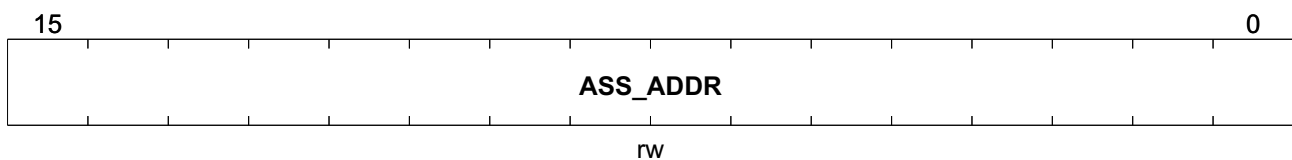
Field	Bits	Type	Description
Res	15:10	ro	Reserved

Registers Description

Field	Bits	Type	Description
LTBR	9	ro	<b>Learning Table Bist Result</b> 0 <sub>B</sub> Works 1 <sub>B</sub> Doesn't Work
LLTBR	8	ro	<b>Linklist Table Bist Result</b> (Linklist Table does not do bist test in normal mode) 0 <sub>B</sub> Works 1 <sub>B</sub> Doesn't Work
CTBR	7	ro	<b>Control Table Bist Result</b> 0 <sub>B</sub> Works 1 <sub>B</sub> Doesn't Work
HITBR	6	ro	<b>Hardware IGMP Table Bist Result</b> 0 <sub>B</sub> Works 1 <sub>B</sub> Doesn't Work
DBBR	5	ro	<b>Data Buffer Bist Result</b> 0 <sub>B</sub> Works 1 <sub>B</sub> Doesn't Work
P5M	4:3	ro	<b>P5 Mode</b> 00 <sub>B</sub> GPSI 01 <sub>B</sub> RMII 10 <sub>B</sub> MII
P4M	2:1	ro	<b>P4 Mode</b> 00 <sub>B</sub> Port 4 uses inner PHY 01 <sub>B</sub> Port 4 uses MII 11 <sub>B</sub> Port 4 isolated PHY
CFG	0	ro	<b>CFG</b>

Assign Address [15:0] Register

AA1	Offset	Reset Value
Assign Address [15:0] Register	132 <sub>H</sub>	0000 <sub>H</sub>



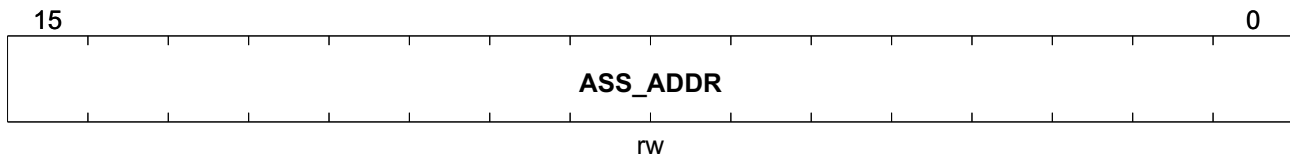
Field	Bits	Type	Description
ASS_ADDR	15:0	rw	Assign Address [15:0]

Assign Address [31:16] Register



**Assign Address [47:32] Register**

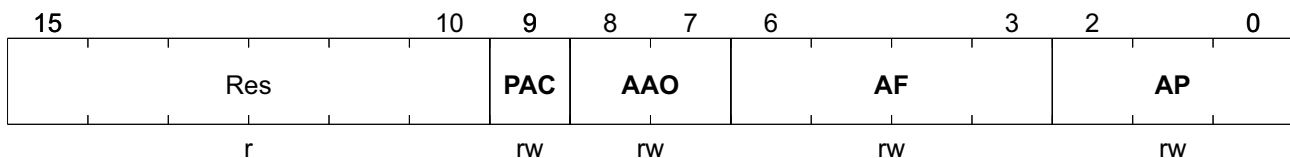
**AA3** **Offset**  
Assign Address [47:32] Register **134<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
ASS_ADDR	15:0	rw	Assign Address [47:32]

**Assign Option Register**

**AO** **Offset**  
Assign Option Register **135<sub>H</sub>** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
Res	15:10	r	<b>Reserved</b>
PAC	9	rw	<p><b>Pause Address Change</b></p> <p>It is useful only when assigned address is used for PAUSE source address</p> <p>0<sub>B</sub> All the ports use this assigned address as the source address of the PAUSE commands</p> <p>1<sub>B</sub> Port 0 uses {assigned address[47:3], 000<sub>B</sub>} as the source address of the PAUSE commands. Port 1 uses {assigned address[47:3], 001<sub>B</sub>} as the source address of the PAUSE commands. Port 2 uses {assigned address[47:3], 010<sub>B</sub>} as the source address of the PAUSE commands. Port 3 uses {assigned address[47:3], 011<sub>B</sub>} as the source address of the PAUSE commands. Port 4 uses {assigned address[47:3], 100<sub>B</sub>} as the source address of the PAUSE commands. Port 5 uses {assigned address[47:3], 101<sub>B</sub>} as the source address of the PAUSE commands.</p>

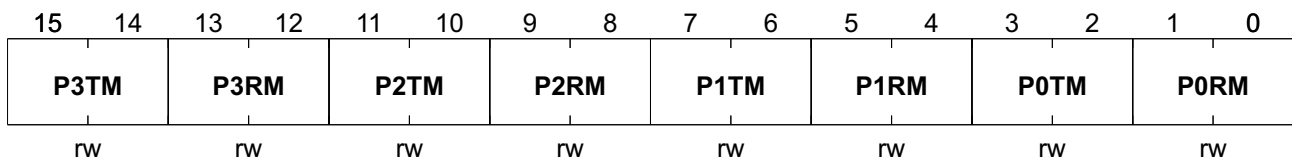


Registers Description

Field	Bits	Type	Description
AAO	8:7	rw	<b>Assign Address Option</b> 00 <sub>B</sub> Assigned address is useless 01 <sub>B</sub> Assigned address is used for PAUSE source address 10 <sub>B</sub> Assigned address is used for assigned lock address or the monitor address 11 <sub>B</sub> Assigned address is used for PAUSE source address
AF	6:3	rw	<b>Assign Fid</b> It is used for to assign lock FID.
AP	2:0	rw	<b>Assign Port</b> It is used for the port that the user wants to assign or for the monitor port.

Mirror Register 0

MIRR0 Offset  
Mirror Register 0 136<sub>H</sub> Reset Value  
0000<sub>H</sub>



Field	Bits	Type	Description
P3TM	15:14	rw	<b>Port 3 Transmit Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0TM</a> for more details.
P3RM	13:12	rw	<b>Port 3 Receive Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0RM</a> for more details.
P2TM	11:10	rw	<b>Port 2 Transmit Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0TM</a> for more details.
P2RM	9:8	rw	<b>Port 2 Receive Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0RM</a> for more details.
P1TM	7:6	rw	<b>Port 1 Transmit Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0TM</a> for more details.
P1RM	5:4	rw	<b>Port 1 Receive Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">P0RM</a> for more detail.
P0TM	3:2	rw	<b>Port 0 Transmit Mirror Option</b> 00 <sub>B</sub> Does not be mirrored 01 <sub>B</sub> The traffic transmitted from Port 0 is mirrored 10 <sub>B</sub> The traffic with DA = assign address transmitted from Port 0 is mirrored 11 <sub>B</sub> The traffic with SA = assign address transmitted from Port 0 is mirrored

Registers Description

Field	Bits	Type	Description
PORM	1:0	rw	<b>Port 0 Receive Mirror Option</b> 00 <sub>B</sub> Does not be mirrored 01 <sub>B</sub> The traffic received on Port 0 is mirrored 10 <sub>B</sub> The traffic with DA = assign address received on Port 0 is mirrored 11 <sub>B</sub> The traffic with SA = assign address received on Port 0 is mirrored

Mirror Register 1

**MIRR1** **Offset** **Reset Value**  
 Mirror Register 1 **137<sub>H</sub>** **0000<sub>H</sub>**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
<b>ME</b>	<b>MCA</b>	<b>MRA</b>	<b>MPA</b>	<b>MLA</b>	<b>MSA</b>	Res	<b>ETUP</b>		<b>P5TM</b>	<b>P5RM</b>	<b>P4TM</b>	<b>P4RM</b>			
rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw			

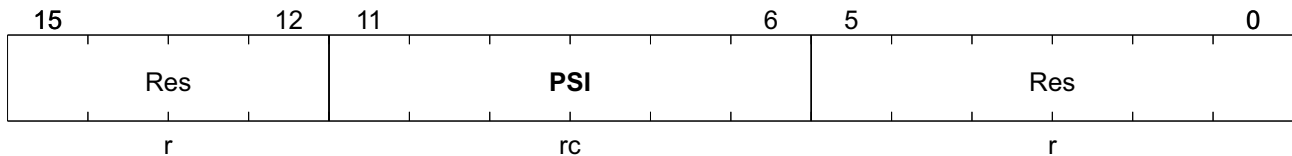
Field	Bits	Type	Description
ME	15	rw	<b>Mirror Enable</b> 0 <sub>B</sub> Disable 1 <sub>B</sub> Enable
MCA	14	rw	<b>Mirror CRC Also</b> 0 <sub>B</sub> Does not mirror 1 <sub>B</sub> Mirrors
MRA	13	rw	<b>Mirror RXER Also</b> 0 <sub>B</sub> Does not mirror 1 <sub>B</sub> Mirrors
MPA	12	rw	<b>Mirror PAUSE Also</b> 0 <sub>B</sub> Does not mirror 1 <sub>B</sub> Mirrors
MLA	11	rw	<b>Mirror Long Also</b> 0 <sub>B</sub> Does not mirror 1 <sub>B</sub> Mirrors
MSA	10	rw	<b>Mirror Short Also</b> 0 <sub>B</sub> Does not mirror 1 <sub>B</sub> Mirrors
Res	9	rw	<b>Reserved</b>
ETUP	8	rw	<b>Enable Transmit Unmonitored Packet to the Mirror Port</b> 0 <sub>B</sub> Mirror port only mirrors the mirrored packets 1 <sub>B</sub> Mirror port also receives packets that are not mirrored but their output ports also contain the mirror port
P5TM	7:6	rw	<b>Port 5 Transmit Mirror Option</b> See register 0136 <sub>H</sub> , <b>POTM</b> for more details.

Registers Description

Field	Bits	Type	Description
P5RM	5:4	rw	<b>Port 5 Receive Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">PORM</a> for more details.
P4TM	3:2	rw	<b>Port 4 Transmit Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">POTM</a> for more details.
P4RM	1:0	rw	<b>Port 4 Receive Mirror Option</b> See register 0136 <sub>H</sub> , <a href="#">PORM</a> for more details.

Security Violation Port

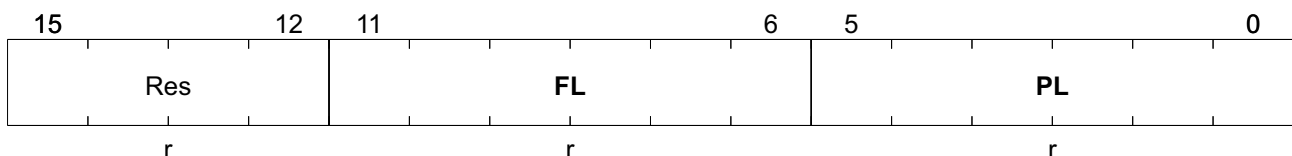
SVP	Offset	Reset Value
Security Violation Port	138 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
Res	15:12	r	<b>Reserved</b>
PSI	11:6	rc	<b>Port Source Intrusion</b> 0 <sub>B</sub> Source Intrusion did not happen 1 <sub>B</sub> Source Intrusion happened
Res	5:0	r	<b>Reserved</b>

Security Status 0

SS0	Offset	Reset Value
Security Status 0	139 <sub>H</sub>	0000 <sub>H</sub>



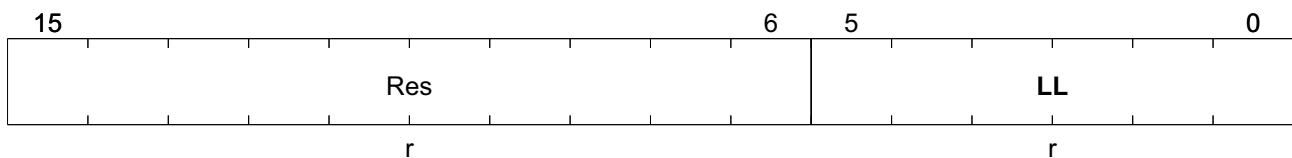
Field	Bits	Type	Description
Res	15:12	r	<b>Reserved</b>
FL	11:6	r	<b>First Lock</b> 0 <sub>B</sub> Port did not lock the address 1 <sub>B</sub> Port locked the address

Registers Description

Field	Bits	Type	Description
PL	5:0	r	<b>Port Locked</b> 0 <sub>B</sub> Port did not close 1 <sub>B</sub> Port closed because of source violation

Security Status 1

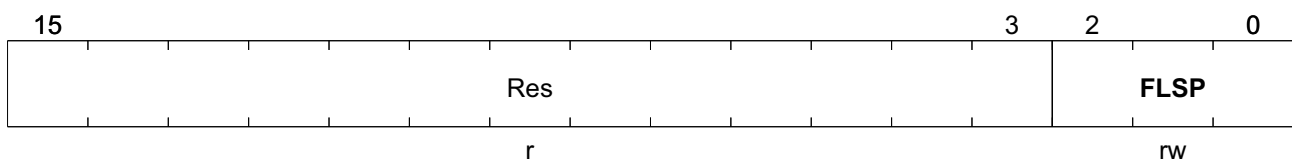
**SS1** **Offset** **Reset Value**  
Security Status 1 13A<sub>H</sub> 0000<sub>H</sub>



Field	Bits	Type	Description
Res	15:6	r	<b>Reserved</b>
LL	5:0	r	<b>Link Lock</b> 0 <sub>B</sub> Link Lock did not happen 1 <sub>B</sub> Link Lock happened

First Lock Address Search

**FLAS** **Offset** **Reset Value**  
First Lock Address Search 13B<sub>H</sub> 0000<sub>H</sub>



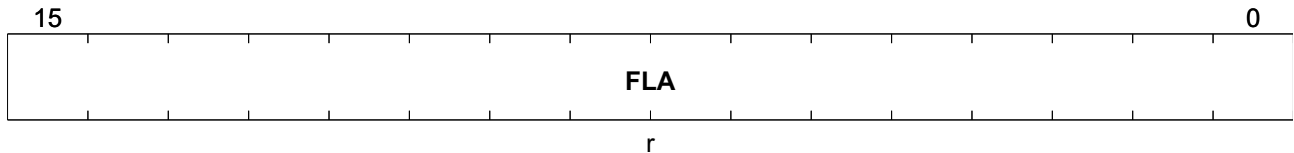
Field	Bits	Type	Description
Res	15:3	r	<b>Reserved</b>

**Registers Description**

<b>Field</b>	<b>Bits</b>	<b>Type</b>	<b>Description</b>
FLSP	2:0	rw	<p><b>First Lock Search Port</b></p> <p>Users could write this register to get the lock address and the lock FID (returned in the 13C<sub>H</sub>, 13D<sub>H</sub>, 13E<sub>H</sub>, 13F<sub>H</sub>) associated with the port.</p> <p>000<sub>B</sub> Search the address and FID locked on the port 0</p> <p>001<sub>B</sub> Search the address and FID locked on the port 1</p> <p>010<sub>B</sub> Search the address and FID locked on the port 1</p> <p>011<sub>B</sub> Search the address and FID locked on the port 1</p> <p>100<sub>B</sub> Search the address and FID locked on the port 1</p> <p>101<sub>B</sub> Search the address and FID locked on the port 1</p>

**First Lock Address [15:0]**

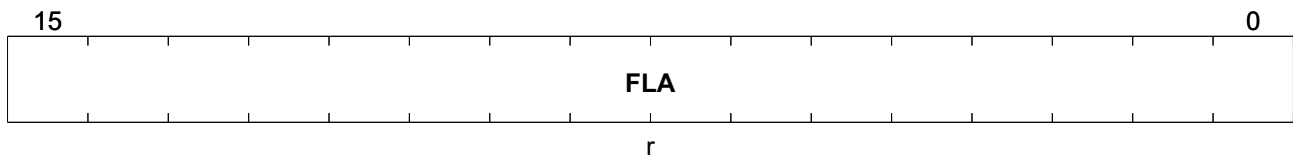
<b>FLA1</b>	<b>Offset</b>	<b>Reset Value</b>
First Lock Address [15:0]	13C <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
FLA	15:0	r	First Lock Address [15:0]

**First Lock Address [31:16]**

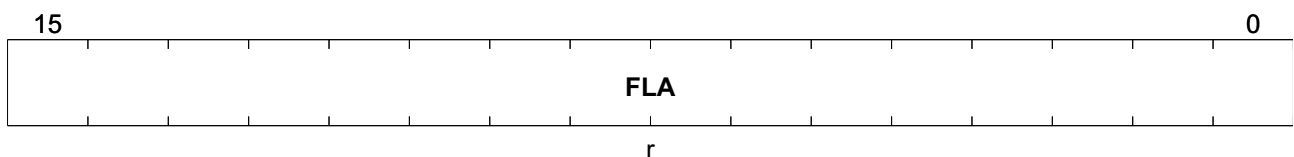
<b>FLA2</b>	<b>Offset</b>	<b>Reset Value</b>
First Lock Address [31:16]	13D <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
FLA	15:0	r	First Lock Address [31:16]

**First Lock Address [47:32]**

<b>FLA3</b>	<b>Offset</b>	<b>Reset Value</b>
First Lock Address [47:32]	13E <sub>H</sub>	0000 <sub>H</sub>

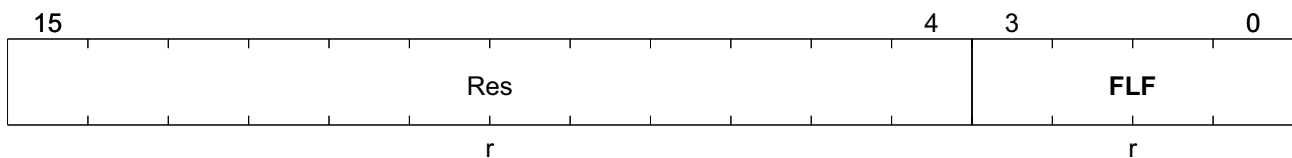


Registers Description

Field	Bits	Type	Description
FLA	15:0	r	First Lock Address [47:32]

First Lock FID

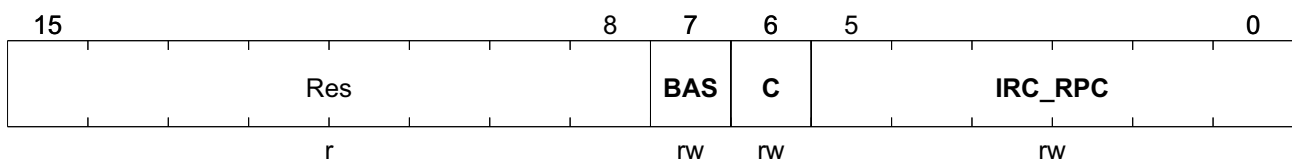
<b>FLF</b>	<b>Offset</b>	<b>Reset Value</b>
First Lock FID	13F <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
Res	15:4	r	Reserved
FLF	3:0	r	First Lock FID

Counter Control Low Register

<b>CCL</b>	<b>Offset</b>	<b>Reset Value</b>
Counter Control Low Register	140 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
Res	15:8	r	Reserved
BAS	7	rw	<b>Busy/Access Start</b> 0 <sub>B</sub> The counter control is free 1 <sub>B</sub> The counter control is busy, or users should write 1 <sub>B</sub> into this bit to start the access when the engine is free
C	6	rw	<b>Counter</b> 0 <sub>B</sub> Indirect Read Counter 1 <sub>B</sub> Renew Port Counter

Registers Description

Field	Bits	Type	Description
IRC_RPC	5:0	rw	<b>Indirect Read Counter</b> It means the counter address <b>Renew Port Counter</b> It means the counters on each port to renew



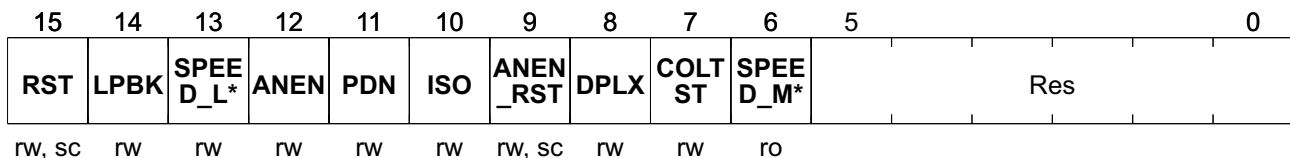


Field	Bits	Type	Description
COUNTER	15:0	r	Counter [31:16]

## 4.4 PHY Registers

### PHY Control Register of Port 0

PHY_C0	Offset	Reset Value
PHY Control Register of Port 0	200 <sub>H</sub>	3100 <sub>H</sub>



Field	Bits	Type	Description
RST	15	rw, sc	<p><b>RESET</b></p> <p>Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values. The software reset process takes <math>25 \leq t_{rs} \leq 25 \mu s</math> to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.</p> <p>0<sub>B</sub> Normal operation 1<sub>B</sub> PHY Reset</p>
LPBK	14	rw	<p><b>Loop Back Enable</b></p> <p>This bit controls the PHY loopback operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit 12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13 of this register.</p> <p>0<sub>B</sub> Disable Loopback mode 1<sub>B</sub> Enable loopback mode</p>
SPEED_LSB	13	rw	<p><b>Speed Selection LSB, 0.6, 0.13</b></p> <p>Link speed is selected by this bit or by auto negotiation if bit 12 of this register is set (in which case, the value of this bit is ignored). If it is fiber mode, 0.13 is always 1. Any write to this bit will have no effect.</p> <p>00<sub>B</sub> 10 Mbit/s 01<sub>B</sub> 100 Mbit/s 10<sub>B</sub> 1000 Mbit/s 11<sub>B</sub> Reserved</p>

Registers Description

Field	Bits	Type	Description
ANEN	12	rw	<p><b>Auto Negotiation Enable</b></p> <p>This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the RECANEN pin detects a logic 1 input level in Twisted-Pair Mode. If it is set when fiber mode is configured, any write to this bit will be ignored .</p> <p>0<sub>B</sub> Disable Auto negotiation process 1<sub>B</sub> Enable auto negotiation process</p>
PDN	11	rw	<p><b>Power Down Enable</b></p> <p>Setting this bit high puts the PHY into power down mode. During the power down mode, TXP/TXN and all LED outputs are tristated and the MII interfaces are isolated.</p> <p>0<sub>B</sub> Normal Operation 1<sub>B</sub> Power Down</p>
ISO	10	rw	<p><b>Isolate PHY from Network</b></p> <p>Setting this control bit isolates the part from the MII, with the exception of the serial management interface. When this bit is asserted, the PHY does not respond to TXD, TXEN and TXER inputs, and it presents a high impedance on its TXC, RXC, CRSDV, RXER, RXD , COL and CRS outputs.</p> <p>0<sub>B</sub> Normal Operation 1<sub>B</sub> Isolate PHY from MII</p>
ANEN_RST	9	rw, sc	<p><b>Restart Auto Negotiation</b></p> <p>Setting this bit while auto negotiation is enabled it forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced.</p> <p>0<sub>B</sub> Normal Operation 1<sub>B</sub> Restart Auto Negotiation Process</p>
DPLX	8	rw	<p><b>Duplex Mode</b></p> <p>If auto negotiation is disabled, this bit determines the duplex mode for the link.</p> <p>0<sub>B</sub> Half Duplex mode 1<sub>B</sub> Full Duplex mode</p>
COLTST	7	rw	<p><b>Collision Test</b></p> <p>When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.</p> <p>0<sub>B</sub> Disable COL signal test 1<sub>B</sub> Enable COL signal test</p>
SPEED_MSB	6	ro	<p><b>Speed Selection MSB</b></p> <p>Set to 0 all the time to indicate that the PHY does not support 1000 Mbit/s function.</p>

**Similar Registers**

All PHY\_Cx registers have the same structure and characteristics, see [PHY\\_C0](#).  
The offset addresses of the other PHY\_Cx registers are listed in [Table 66](#).

**Table 66** PHY\_Cx Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PHY_C1	PHY Control Register of Port 1	220 <sub>H</sub>	
PHY_C2	PHY Control Register of Port 2	240 <sub>H</sub>	
PHY_C3	PHY Control Register of Port 3	260 <sub>H</sub>	
PHY_C4	PHY Control Register of Port 4	280 <sub>H</sub>	



Field	Bits	Type	Description
REM_FLT	4	ro	<b>Remote Fault Detect</b> This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05 <sub>H</sub> ) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read. 0 <sub>B</sub> Remote Fault not detected 1 <sub>B</sub> Remote Fault detected
CAP_ANEG	3	ro	<b>Auto Negotiation Ability</b> TP : This bit is set to 1 all the time, indicating that PHY is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that PHY is not capable of auto negotiation in Fiber Mode. 0 <sub>B</sub> Not capable of auto negotiation 1 <sub>B</sub> Capable of auto negotiation
LINK	2	ro	<b>Link Status</b> This bit reflects the current state of the link – test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status 0 <sub>B</sub> Link is down 1 <sub>B</sub> Link is up
JAB	1	ro	<b>Jabber Detect</b> 0 <sub>B</sub> Jabber condition not detected 1 <sub>B</sub> Jabber condition detected
EXTREG	0	ro	<b>Extended Capability</b> This bit defaults to 1, indicating that the PHY implements extended registers. 0 <sub>B</sub> No extended register set 1 <sub>B</sub> Extended register set

### Similar Registers

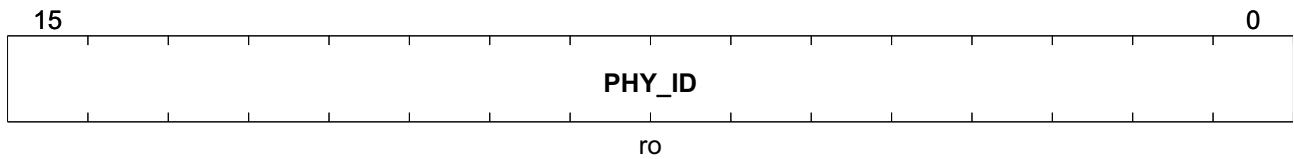
All PHY\_Sx registers have the same structure and characteristics, see [PHY\\_S0](#). The offset addresses of the other PHY\_Sx registers are listed in [Table 67](#).

**Table 67 PHY\_Sx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
PHY_S1	PHY Status Register of Port 1	221 <sub>H</sub>	
PHY_S2	PHY Status Register of Port 2	241 <sub>H</sub>	
PHY_S3	PHY Status Register of Port 3	261 <sub>H</sub>	
PHY_S4	PHY Status Register of Port 4	281 <sub>H</sub>	

### PHY Identifier Register of Port 0 (A)

PHY_I0_A	Offset	Reset Value
PHY Identifier Register of Port 0 (A)	202 <sub>H</sub>	0302 <sub>H</sub>



Field	Bits	Type	Description
PHY_ID	15:0	ro	IEEE Address

### Similar Registers

All PHY\_Ix\_A registers have the same structure and characteristics, see [PHY\\_I0\\_A](#).  
The offset addresses of the other PHY\_Ix\_A registers are listed in [Table 68](#).

**Table 68** PHY\_Ix\_A Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PHY_I1_A	PHY Identifier Register of Port 1 (A)	222 <sub>H</sub>	
PHY_I2_A	PHY Identifier Register of Port 2 (A)	242 <sub>H</sub>	
PHY_I3_A	PHY Identifier Register of Port 3 (A)	262 <sub>H</sub>	
PHY_I4_A	PHY Identifier Register of Port 4 (A)	282 <sub>H</sub>	

### PHY Identifier Register of Port 0 (B)

PHY_I0_B	Offset	Reset Value
PHY Identifier Register of Port 0 (B)	203 <sub>H</sub>	6071 <sub>H</sub>



Field	Bits	Type	Description
PHY_ID	15:10	ro	IEEE Address
Model_ID	9:4	ro	IEEE Model No.
REV_ID	3:0	ro	IEEE Revision No.

### Similar Registers

All PHY\_Ix\_B registers have the same structure and characteristics, see [PHY\\_I0\\_B](#).  
The offset addresses of the other PHY\_Ix\_B registers are listed in [Table 69](#).

**Table 69 PHY\_Ix\_B Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
PHY_I1_B	PHY Identifier Register of Port 1 (B)	223 <sub>H</sub>	
PHY_I2_B	PHY Identifier Register of Port 2 (B)	243 <sub>H</sub>	
PHY_I3_B	PHY Identifier Register of Port 3 (B)	263 <sub>H</sub>	
PHY_I4_B	PHY Identifier Register of Port 4 (B)	283 <sub>H</sub>	

**Auto Negotiation Advertisement Register of Port 0**

<b>ANAP0</b>	<b>Offset</b>	<b>Reset Value</b>
<b>Auto Negotiation Advertisement Register of Port 0</b>	<b>204<sub>H</sub></b>	<b>05E1<sub>H</sub></b>

15	14	13	12	11	10	9	8	7	6	5	4	0	
NP	Res	RF	Res	ASM_DIR	PAUSE	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	SF		
ro		ro		rw	rw	ro	rw	rw	rw	rw		ro	

Field	Bits	Type	Description
NP	15	ro	<b>Next Page</b> This bit defaults to 1, indicating that PHY is next page capable
RF	13	ro	<b>Remote Fault</b> This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner. 0 <sub>B</sub> No remote fault has been detected 1 <sub>B</sub> Remote Fault has been detected
ASM_DIR	11	rw	<b>Asymmetric Pause Direction</b> Bit[ 11:10 ] Capability 00 <sub>B</sub> No Pause 01 <sub>B</sub> Symmetric PAUSE 10 <sub>B</sub> Asymmetric PAUSE toward Link Partner 11 <sub>B</sub> Both Symmetric PAUSE and Asymmetric PAUSE toward local device
PAUSE	10	rw	<b>Pause Operation for Full Duplex</b> Value on PAUREC will be stored in this bit during power on reset.
T4	9	ro	<b>Technology Ability for 100Base-T4</b> Defaults to 0.
TX_FDX	8	rw	<b>100Base-TX Full Duplex</b> 0 <sub>B</sub> Not capable of 100M Full duplex operation 1 <sub>B</sub> Capable of 100M Full duplex operation



Registers Description

Field	Bits	Type	Description
TX_HDX	7	rw	<b>100Base-TX Half Duplex</b> 0 <sub>B</sub> Not capable of 100M operation 1 <sub>B</sub> Capable of 100M operation
10_FDX	6	rw	<b>10BASE-T Full Duplex</b> 0 <sub>B</sub> Not capable of 10M full duplex operation 1 <sub>B</sub> Capable of 10M Full Duplex operation
10_HDX	5	rw	<b>10Base-T Half Duplex</b> <i>Note: Bit 8:5 should be combined with REC100, RECFUL pin input to determine the finalized speed and duplex mode.</i> 0 <sub>B</sub> Not capable of 10M operation 1 <sub>B</sub> Capable of 10M operation
SF	4:0	ro	<b>Selector Field</b> These 5 bits are hardwired to 00001 <sub>B</sub> , indicating that the PHY supports IEEE 802.3 CSMA/CD.

**Similar Registers**

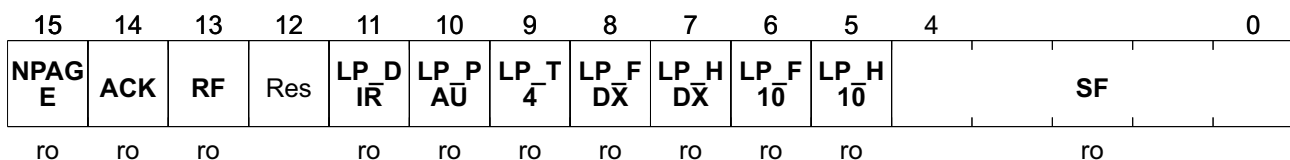
All ANAPx registers have the same structure and characteristics, see [ANAP0](#).  
The offset addresses of the other ANAPx registers are listed in [Table 70](#).

**Table 70 ANAPx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
ANAP1	Auto Negotiation Advertisement Register of Port 1	224 <sub>H</sub>	
ANAP2	Auto Negotiation Advertisement Register of Port 2	244 <sub>H</sub>	
ANAP3	Auto Negotiation Advertisement Register of Port 3	264 <sub>H</sub>	
ANAP4	Auto Negotiation Advertisement Register of Port 4	284 <sub>H</sub>	

**Auto Negotiation Link Partner Ability Register of Port 0**

**ANLPA0** **Offset**  
Auto Negotiation Link Partner Ability **205<sub>H</sub>**  
Register of Port 0 **Reset Value**  
**01E1<sub>H</sub>**



Field	Bits	Type	Description
NPAGE	15	ro	<b>Next Page</b> 0 <sub>B</sub> Not capable of next page function 1 <sub>B</sub> Capable of next page function

Registers Description

Field	Bits	Type	Description
ACK	14	ro	<b>Acknowledge</b> 0 <sub>B</sub> Not acknowledged 1 <sub>B</sub> Link Partner acknowledges reception of the ability data word
RF	13	ro	<b>Remote Fault</b> 0 <sub>B</sub> No remote fault has been detected 1 <sub>B</sub> Remote Fault has been detected
LP_DIR	11	ro	<b>Link Partner Asymmetric Pause Direction</b>
LP_PAU	10	ro	<b>Link Partner Pause CapabilityValue on PAUREC</b> Will be stored in this bit during power on reset.
LP_T4	9	ro	<b>Link Partner Technology Ability</b> For 100Base-T4Defaults to 0.
LP_FDX	8	ro	<b>100Base-TX Full Duplex</b> 0 <sub>B</sub> Not capable of 100M Full duplex operation 1 <sub>B</sub> Capable of 100M Full duplex operation
LP_HDX	7	ro	<b>100Base-TX Half Duplex</b> 0 <sub>B</sub> Not capable of 100M operation 1 <sub>B</sub> Capable of 100M operation
LP_F10	6	ro	<b>10BASE-T Full Duplex</b> 0 <sub>B</sub> Not capable of 10M full duplex operation 1 <sub>B</sub> Capable of 10M Full Duplex operation
LP_H10	5	ro	<b>10Base-T Half Duplex</b> 0 <sub>B</sub> Not capable of 10M operation 1 <sub>B</sub> Capable of 10M operation
SF	4:0	ro	<b>Selector Field</b> Encoding Definitions

**Similar Registers**

All ANLPAx registers have the same structure and characteristics, see [ANLPA0](#).  
The offset addresses of the other ANLPAx registers are listed in [Table 71](#).

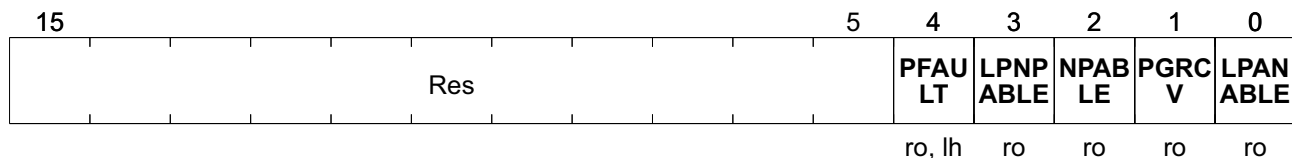
**Table 71 ANLPAx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
ANLPA1	Auto Negotiation Link Partner Ability Register of Port 1	225 <sub>H</sub>	
ANLPA2	Auto Negotiation Link Partner Ability Register of Port 2	245 <sub>H</sub>	
ANLPA3	Auto Negotiation Link Partner Ability Register of Port 3	265 <sub>H</sub>	
ANLPA4	Auto Negotiation Link Partner Ability Register of Port 4	285 <sub>H</sub>	

**Auto Negotiation Expansion Register of Port 0**

Registers Description

**ANE0** **Offset**  
**Auto Negotiation Expansion Register of Port** **206<sub>H</sub>**  
**0** **Reset Value**  
**0000<sub>H</sub>**



Field	Bits	Type	Description
PFAULT	4	ro, lh	<b>Parallel Detection Fault</b> 0 <sub>B</sub> No Fault has been detected 1 <sub>B</sub> Fault has been detected
LPNPABLE	3	ro	<b>Link Partner Next Page Able</b> 0 <sub>B</sub> Link Partner is not next page capable 1 <sub>B</sub> Link Partner is next page capable
NPABLE	2	ro	<b>Next Page Able</b> Defaults to 0, indicating PHY is not capable of next page.
PGRCV	1	ro	<b>Page Received</b> 0 <sub>B</sub> No new page has been received 1 <sub>B</sub> A new page has been received
LPANABLE	0	ro	<b>Link Partner Auto Negotiation Able</b> 0 <sub>B</sub> Link Partner is not auto negotiable 1 <sub>B</sub> Link Partner is auto negotiable

**Similar Registers**

All ANEx registers have the same structure and characteristics, see [ANE0](#).  
The offset addresses of the other ANEx registers are listed in [Table 72](#).

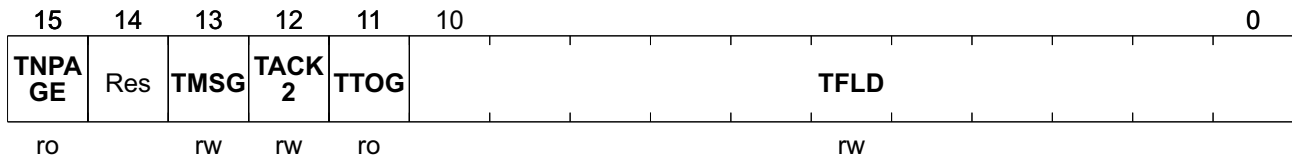
**Table 72 ANEx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
ANE1	Auto Negotiation Expansion Register of Port 1	226 <sub>H</sub>	
ANE2	Auto Negotiation Expansion Register of Port 2	246 <sub>H</sub>	
ANE3	Auto Negotiation Expansion Register of Port 3	266 <sub>H</sub>	
ANE4	Auto Negotiation Expansion Register of Port 4	286 <sub>H</sub>	

**Next Page Transmit Register of Port 0**

**NPT0** **Offset**  
**Next Page Transmit Register of Port 0** **207<sub>H</sub>**  
**Reset Value**  
**2001<sub>H</sub>**

Registers Description



Field	Bits	Type	Description
TNPAGE	15	ro	<b>Transmit Next Page</b> Transmit Code Word Bit 15
TMSG	13	rw	<b>Transmit Message Page</b> Transmit Code Word Bit 13
TACK2	12	rw	<b>Transmit Acknowledge 2</b> Transmit Code Word Bit 12
TTOG	11	ro	<b>Transmit Toggle</b> Transmit Code Word Bit 11
TFLD	10:0	rw	<b>Transmit Message Field</b> Transmit Code Word Bit 10..0

**Similar Registers**

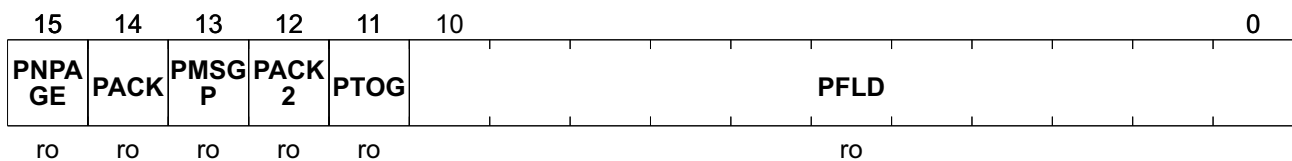
All NPTx registers have the same structure and characteristics, see [NPT0](#).  
The offset addresses of the other NPTx registers are listed in [Table 73](#).

**Table 73 NPTx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
NPT1	Next Page Transmit Register of Port 1	227 <sub>H</sub>	
NPT2	Next Page Transmit Register of Port 2	247 <sub>H</sub>	
NPT3	Next Page Transmit Register of Port 3	267 <sub>H</sub>	
NPT4	Next Page Transmit Register of Port 4	287 <sub>H</sub>	

**Link Partner Next Page Register of Port 0**

<b>LPNP0</b>	<b>Offset</b>	<b>Reset Value</b>
Link Partner Next Page Register of Port 0	208 <sub>H</sub>	0000 <sub>H</sub>



Field	Bits	Type	Description
PNPAGE	15	ro	<b>Link Partner Next Page</b> Receives Code Word Bit 15

Registers Description

Field	Bits	Type	Description
PACK	14	ro	<b>Link Partner Acknowledge</b> Receives Code Word Bit 14
PMSGP	13	ro	<b>Link Partner Message Page</b> Receives Code Word Bit 13
PACK2	12	ro	<b>Link Partner Acknowledge 2</b> Receives Code Word Bit 12
PTOG	11	ro	<b>Link Partner Toggle</b> Receives Code Word Bit 11
PFLD	10:0	ro	<b>Link Partner Message Field</b> Receives Code Word Bit 11

**Similar Registers**

All LPNPx registers have the same structure and characteristics, see [LPNP0](#).  
The offset addresses of the other LPNPx registers are listed in [Table 74](#).

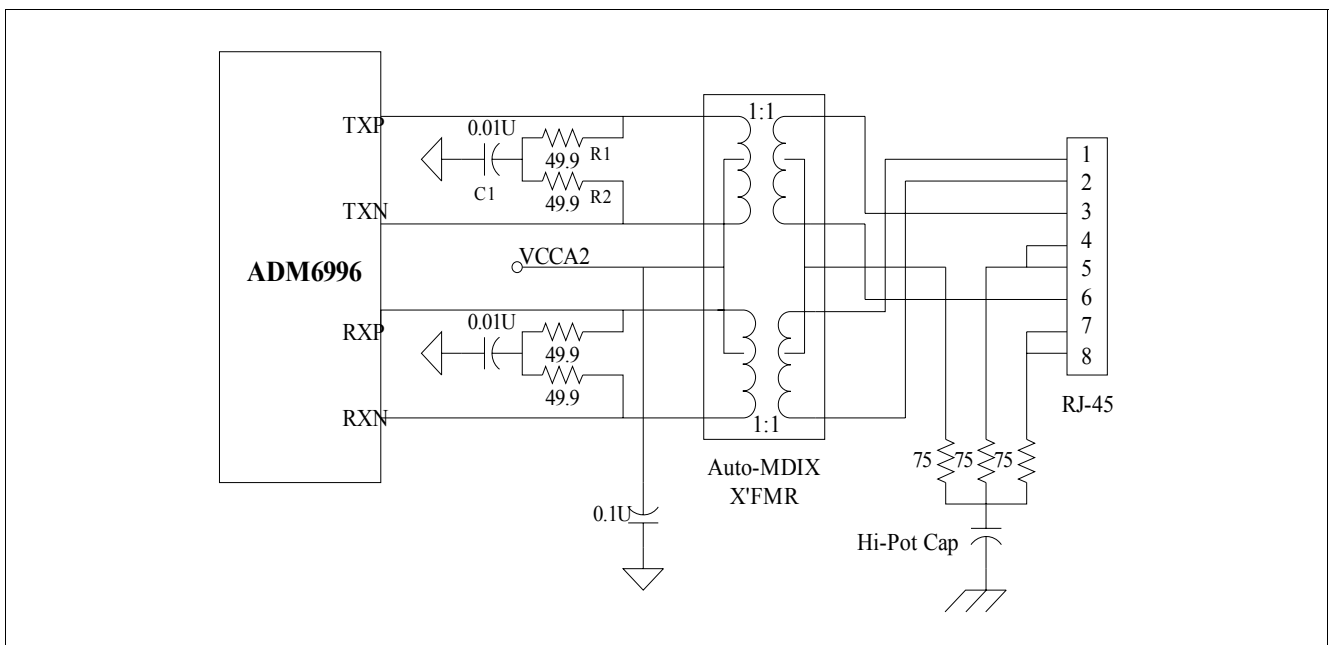
**Table 74 LPNPx Registers**

Register Short Name	Register Long Name	Offset Address	Page Number
LPNP1	Link Partner Next Page Register of Port 1	228 <sub>H</sub>	
LPNP2	Link Partner Next Page Register of Port 2	248 <sub>H</sub>	
LPNP3	Link Partner Next Page Register of Port 3	268 <sub>H</sub>	
LPNP4	Link Partner Next Page Register of Port 4	288 <sub>H</sub>	

## 5 Electrical Specification

### 5.1 TX/FX Interface

#### 5.1.1 TP Interface



**Figure 17 TP Interface**

Transformer requirements:

- TX/RX rate 1:1
- TX/RX central tap connect together to VCCA2

Users can change the TX/RX pin for easy layout but do not change the polarity. Samurai-6M/6MX (ADM6996M/MX) supports auto polarity on the receiving side.

### 5.1.2 FX Interface

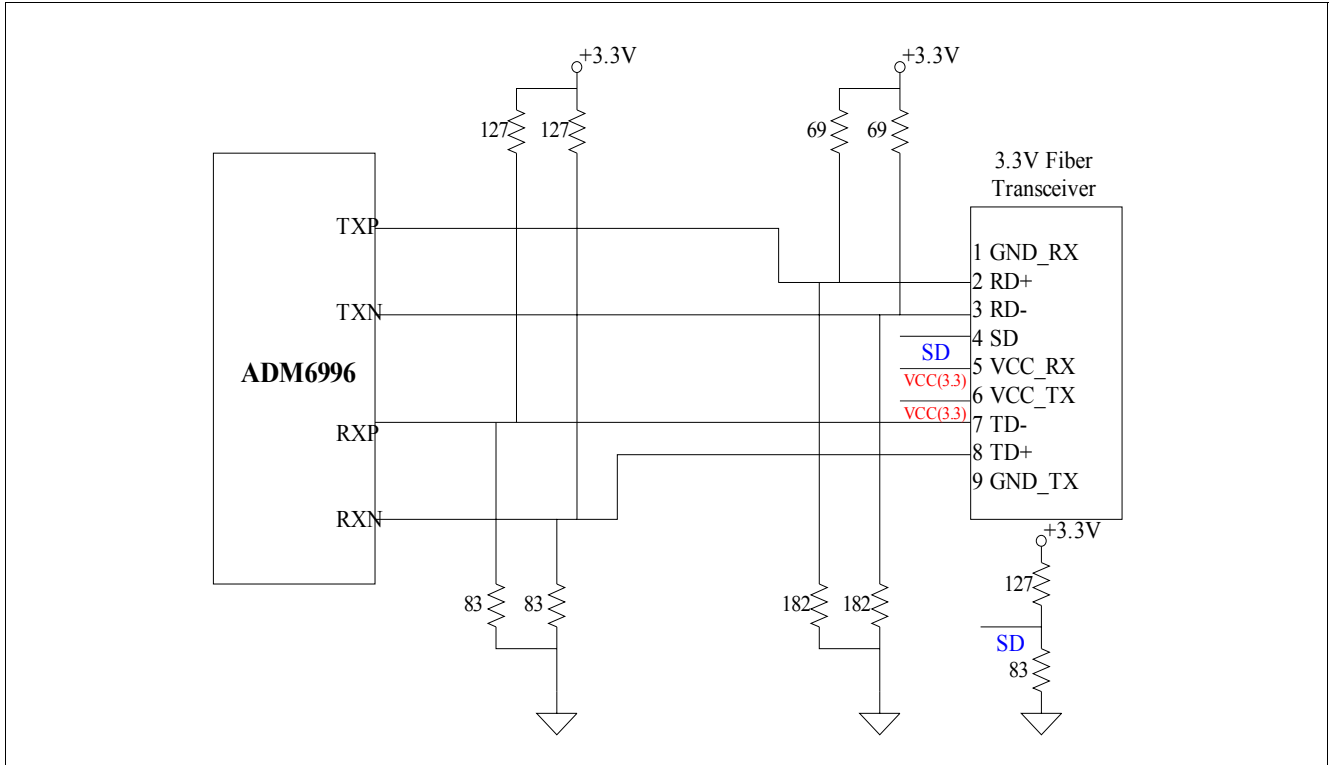


Figure 18 FX Interface

## 5.2 DC Characterization

Table 75 Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power consumption when all twisted pair ports are linked at 100 Mbit/s.	$P_{100M\_5TP}$	—	980	—	mW	Under EEPROM Register 29 <sub>H</sub> = C000 <sub>H</sub> , and 30 <sub>H</sub> = 985 <sub>H</sub>
Power consumption when all twisted pair ports are linked at 10 Mbit/s (include transformer).	$P_{10M\_5TP}$	—	1450	—	mW	Under EEPROM Register 29 <sub>H</sub> = C000 <sub>H</sub> , and 30 <sub>H</sub> = 985 <sub>H</sub>
Power consumption when all twisted pair ports are disconnected.	$P_{DIS\_5TP}$	—	500	—	mW	Under EEPROM Register 29 <sub>H</sub> = C000 <sub>H</sub> , and 30 <sub>H</sub> = 985 <sub>H</sub>

**Table 76 Absolute Maximum Ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply for I/O pad	$V_{CC30}$	2.97	3.3	3.63	V	–
3.3 V Power Supply for bias circuit	$V_{CCBS}$	2.97	3.3	3.63	V	–
3.3 V Power Supply for A/D converter	$V_{CCAD}$	2.97	3.3	3.63	V	–
1.8 V Power Supply for line driver	$V_{CCA2}$	1.62	1.8	1.98	V	–
1.8 V Power Supply for PLL	$V_{CCPLL}$	1.62	1.8	1.98	V	–
1.8 V Power Supply for Digital core	$V_{CCIK}$	1.62	1.8	1.98	V	–
Input Voltage	$V_{IN}$	-0.3	–	$V_{CC30} + 0.3$	V	–
Output Voltage	$V_{out}$	-0.3	–	$V_{CC30} + 0.3$	V	–
Maximum current for 3.3 V power supply	$I_{3.3VMAX}$	–	–	100	mA	–
Maximum current for 1.8 V power supply (include transformer)	$I_{1.8VMAX}$	–	–	800	mA	–
Storage Temperature	$T_{STG}$	-55	–	155	°C	–
Thermal Resistance	$\theta_{JA}$		33.0		°C/W	
	$\theta_{JC}$		14.9		°C/W	
ESD Rating	$ESD$	1.0	–	–	kV	–

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

**Table 77 Recommended Operating Conditions**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply for I/O pad	$V_{CC30}$	3.135	3.3	3.465	V	–
3.3 V Power Supply for bias circuit	$V_{CCBS}$	3.135	3.3	3.465	V	–
3.3 V Power Supply for A/D converter	$V_{CCAD}$	3.135	3.3	3.465	V	–
1.8 V Power Supply for line driver	$V_{CCA2}$	1.71	1.8	1.89	V	–
1.8 V Power Supply for PLL	$V_{CCPLL}$	1.71	1.8	1.89	V	–
1.8 V Power Supply for Digital core	$V_{CCIK}$	1.71	1.8	1.89	V	–



**Table 77 Recommended Operating Conditions (cont'd)**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage	$V_{in}$	0	–	$V_{CC}$	V	–
Junction Operating Temperature	$T_j$	0	25	115	°C	–

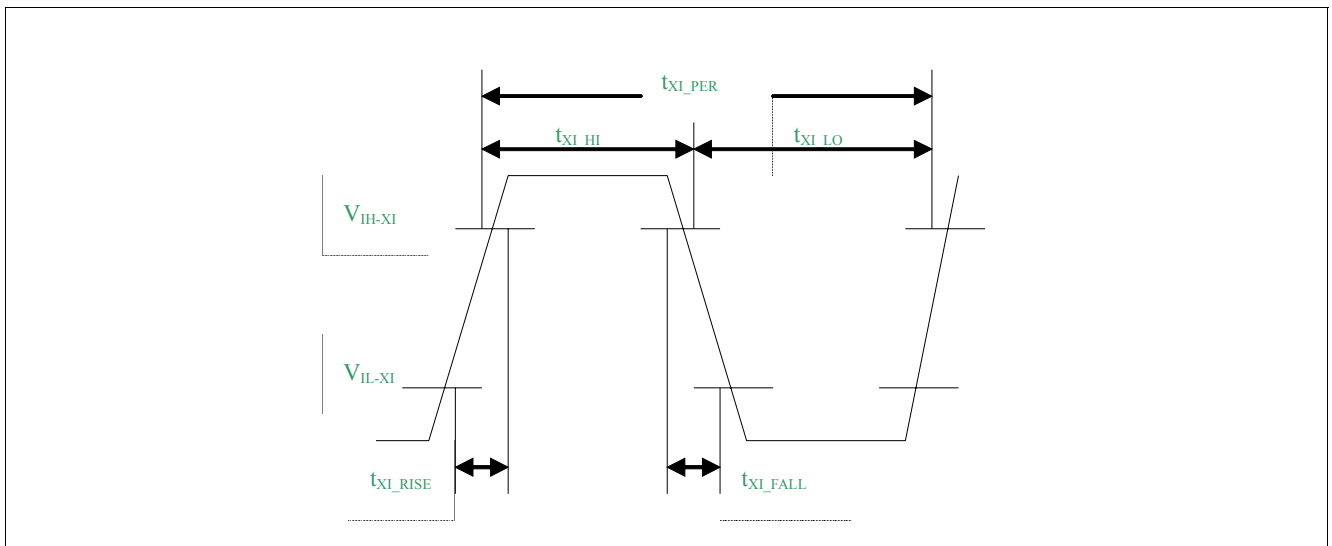
**Table 78 DC Electrical Characteristics for 3.3 V Operation<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	$V_{IL}$	–	–	0.8	V	TTL
Input High Voltage	$V_{IH}$	2.0	–	–	V	TTL
Output Low Voltage	$V_{OL}$	–	–	0.4	V	TTL
Output High Voltage	$V_{OH}$	2.4	–	–	V	TTL
Input Pull-up/down Resistance	$R_i$	–	50	–	kΩ	$V_{IL} = 0\text{ V}$ or $V_{IH} = V_{cc3o}$

1) Under  $V_{CC3O} = 2.97\text{V} \sim 3.63\text{V}$ ,  $T_j = 0\text{ °C} \sim 115\text{ °C}$

## 5.3 AC Characterization

### 5.3.1 XTAL/OSC Timing

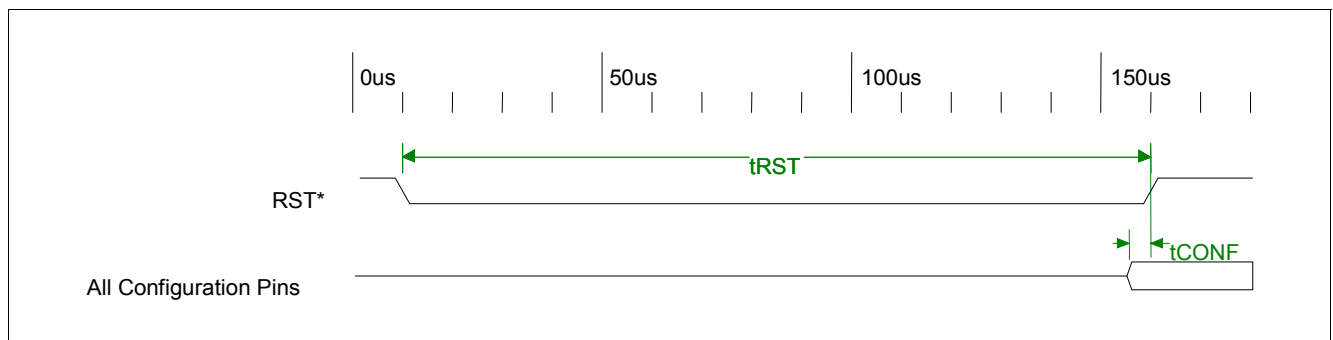


**Figure 19 XTAL/OSC Timing**

**Table 79 XTAL/OSC Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period	$t_{\_XI\_PER}$	40.0 - 50ppm	40.0	40.0 + 50ppm	ns	–
XI/OSCI Clock High	$t_{\_XI\_HI}$	14	20.0	–	ns	–
XI/OSCI Clock Low	$t_{\_XI\_LO}$	14	20.0	–	ns	–
XI/OSCI Clock Rise Time, $V_{IL}$ (max) to $V_{IH}$ (min.)	$t_{\_XI\_RISE}$	–	–	4	ns	–
XI/OSCI Clock Fall Time, $V_{IH}$ (min.) to $V_{IL}$ (max)	$t_{\_XI\_FALL}$	–	–	4	ns	–

### 5.3.2 Power On Reset



**Figure 20 Power On Reset Timing**

**Table 80 Power On Reset Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	$t_{RST}$	100	–	–	ms	–
Start of Idle Pulse Width	$t_{CONF}$	100	–	–	ns	–

### 5.3.3 EEPROM Interface Timing

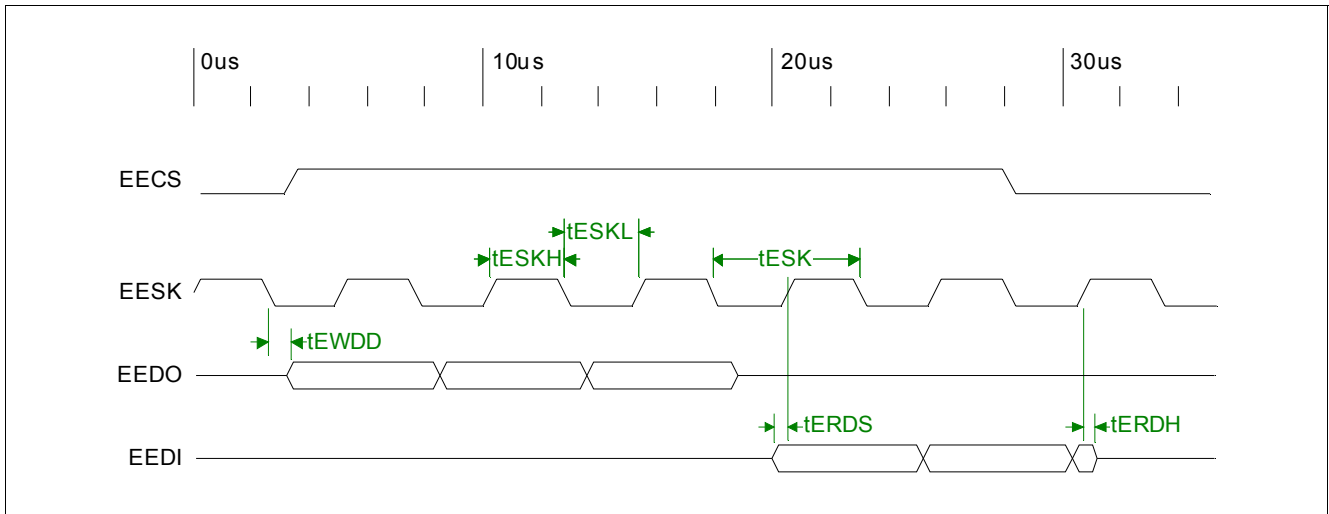


Figure 21 EEPROM Interface Timing

Table 81 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	$t_{ESK}$	–	5120	–	ns	–
EESK Low Period	$t_{ESKL}$	2550	–	2570	ns	–
EESK High Period	$t_{ESKH}$	2550	–	2570	ns	–
EEDI to EESK Rising Setup Time	$t_{ERDS}$	10	–	–	ns	–
EEDI to EESK Rising Hold Time	$t_{ERDH}$	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	$t_{EWDD}$	–	–	20	ns	–

### 5.3.4 10Base-TX MII Input Timing

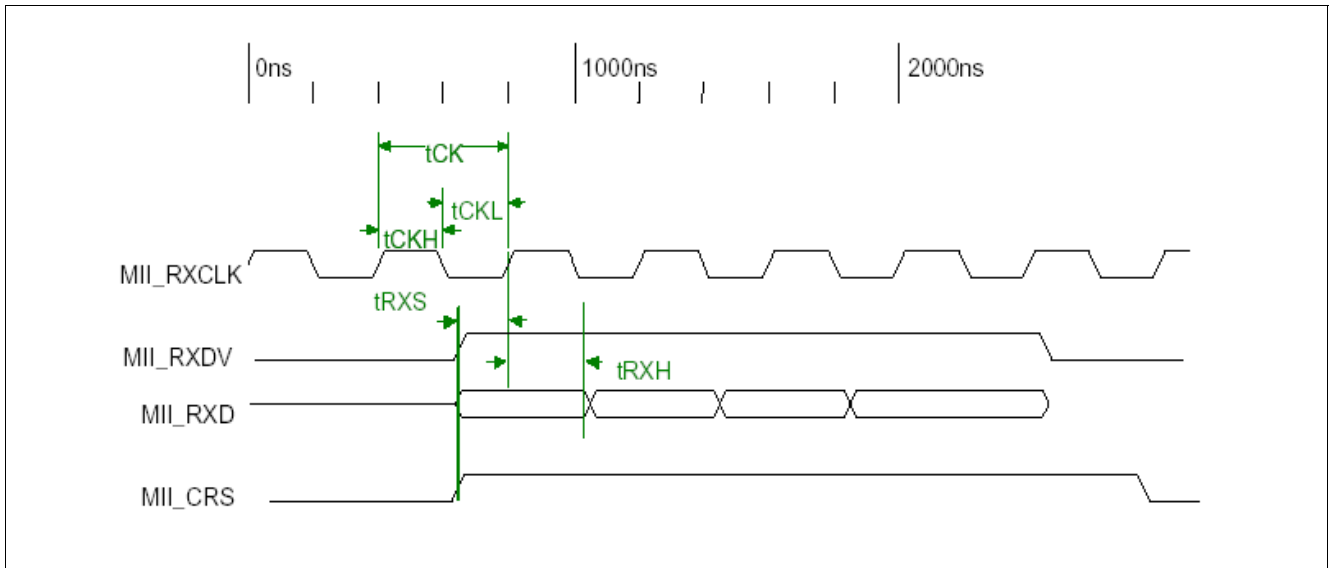


Figure 22 10Base-TX MII Input Timing

Table 82 10Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	$t_{CK}$	–	400	–	ns	–
MII_RXCLK Low Period	$t_{CKL}$	180	–	220	ns	–
MII_RXCLK High Period	$t_{CKH}$	180	–	220	ns	–
MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising setup	$t_{RXS}$	10	–	–	ns	–
MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising hold	$t_{RXH}$	10	–	–	ns	–

### 5.3.5 10Base-TX MII Output Timing

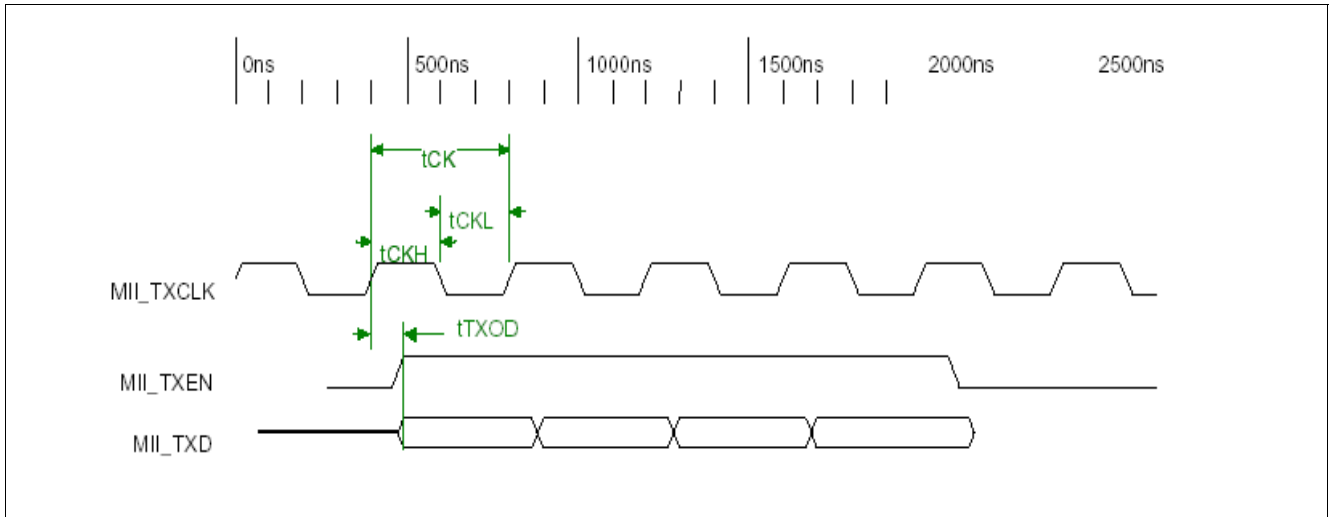


Figure 23 10Base-TX MII Output Timing

Table 83 10-Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	$t_{CK}$	–	400	–	ns	–
MII_TXCLK Low Period	$t_{CKL}$	180	–	220	ns	–
MII_TXCLK High Period	$t_{CKH}$	180	–	220	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	$t_{TXOD}$	0	–	25	ns	–

### 5.3.6 100Base-TX MII Input Timing

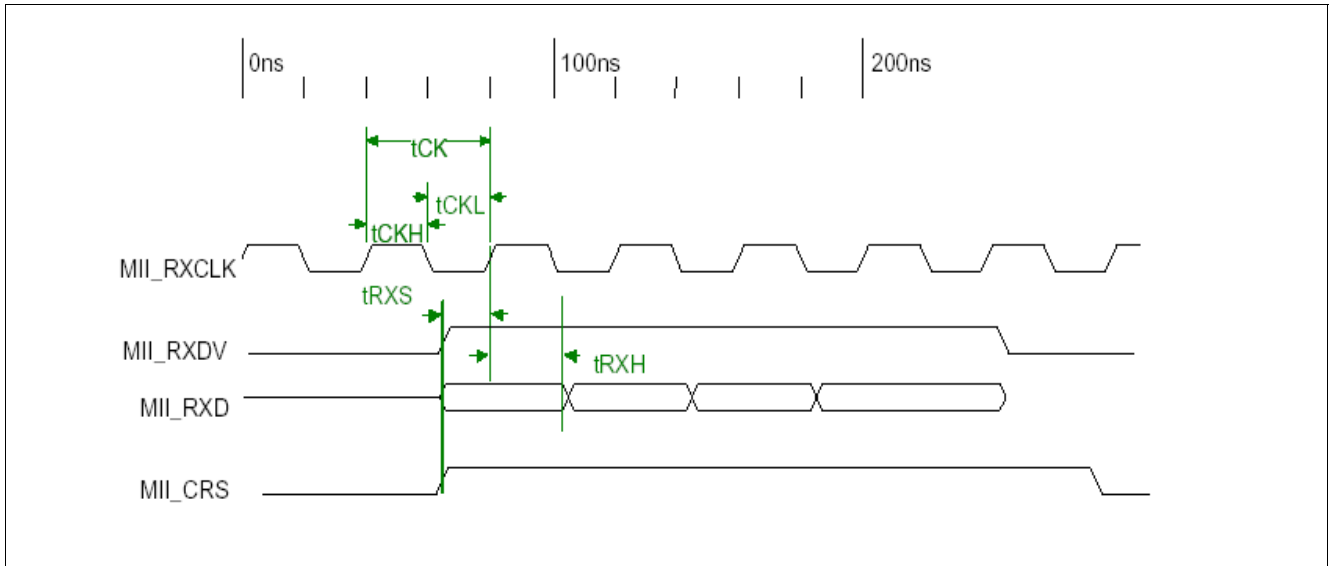


Figure 24 100Base-TX MII Input Timing

Table 84 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	$t_{CK}$	–	40	–	ns	–
MII_RXCLK Low Period	$t_{CKL}$	18	–	22	ns	–
MII_RXCLK High Period	$t_{CKH}$	18	–	22	ns	–
MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising setup	$t_{RXS}$	10	–	–	ns	–
MII_CRD, MII_RXDV and MII_RXD to MII_RXCLK rising hold	$t_{RXH}$	10	–	–	ns	–

### 5.3.7 100Base-TX MII Output Timing

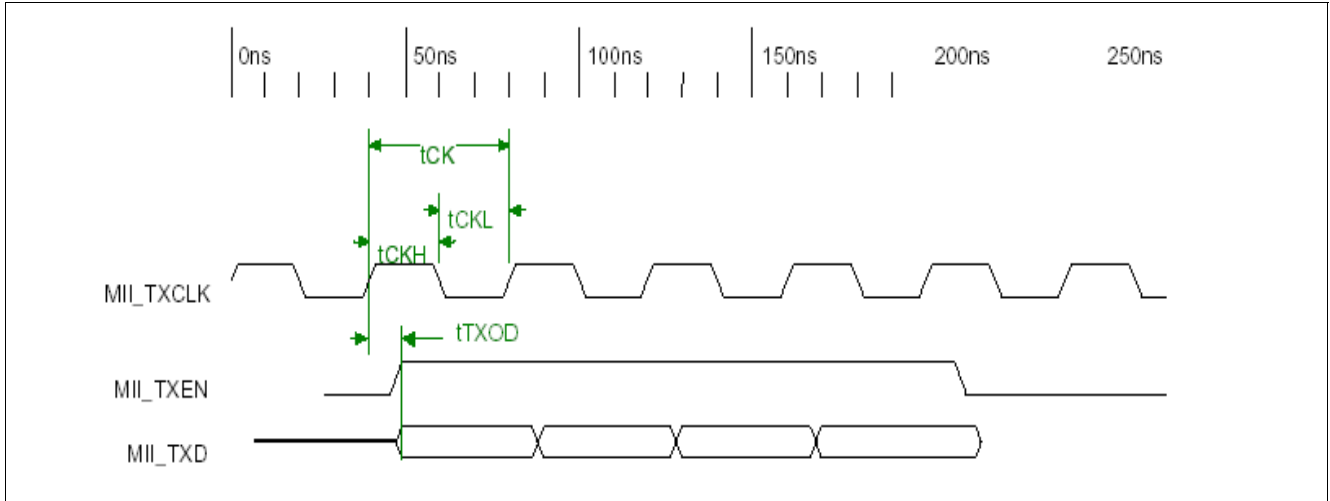


Figure 25 100Base-TX MII Output Timing

Table 85 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	$t_{CK}$	–	40	–	ns	–
MII_TXCLK Low Period	$t_{CKL}$	18	–	22	ns	–
MII_TXCLK High Period	$t_{CKH}$	18	–	22	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	$t_{TXOD}$	0	–	25	ns	–

### 5.3.8 RMII REFCLK Input Timing

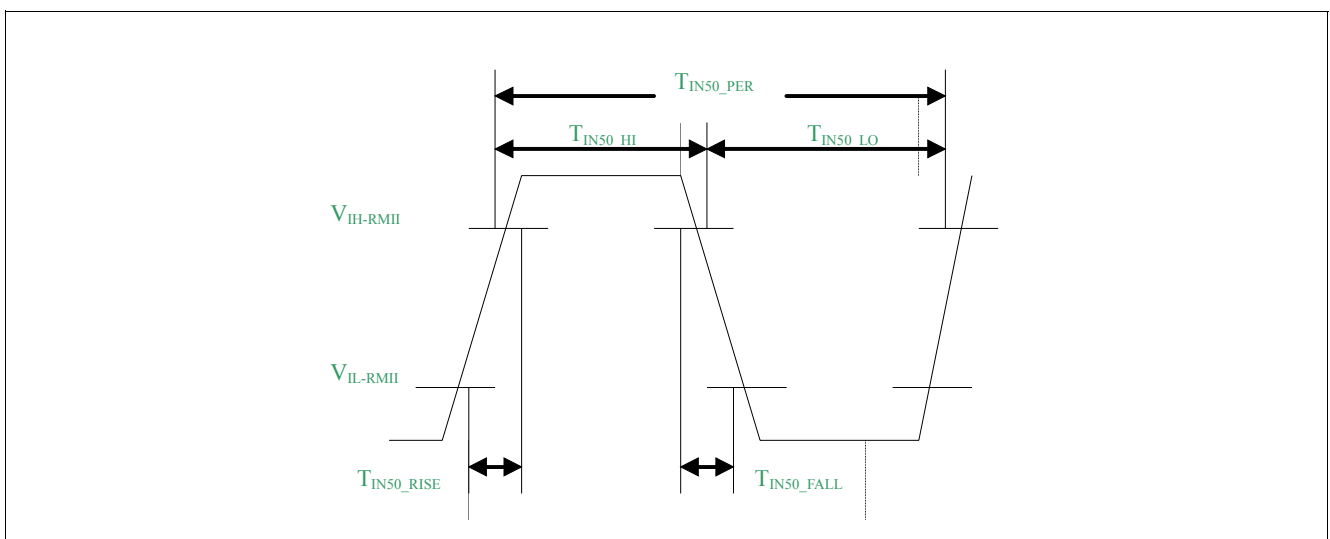
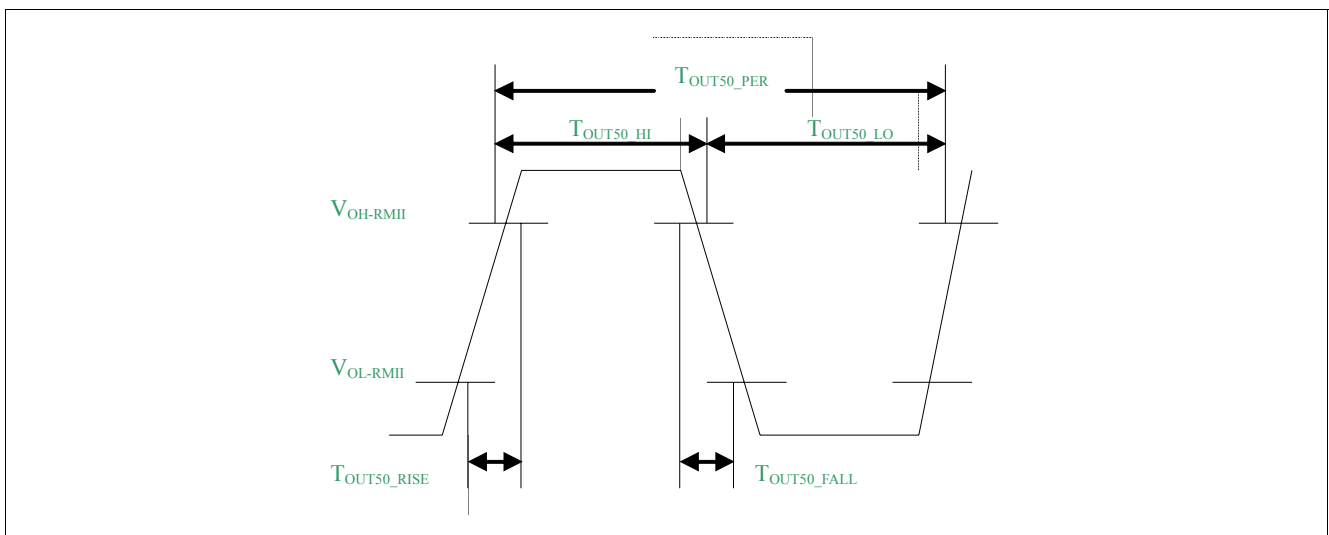


Figure 26 RMII REFCLK Input Timing

**Table 86 RMI REFCLK Input Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	$t_{IN50\_PER}$	40.0 - 50ppm	40.0	40.0 + 50ppm	ns	–
REFCLK Clock High	$t_{IN50\_HI}$	14	20.0	–	ns	–
REFCLK Clock Low	$t_{IN50\_LO}$	14	20.0	–	ns	–
REFCLK Clock Rise Time, $V_{IL}$ (max) to $V_{IH}$ (min.)	$t_{IN50\_RISE}$	–	–	2	ns	–
REFCLK Clock Fall Time, $V_{IH}$ (min.) to $V_{IL}$ (max)	$t_{IN50\_FALL}$	–	–	2	ns	–

### 5.3.9 RMI REFCLK Output Timing



**Figure 27 RMI REFCLK Output Timing**

**Table 87 RMI REFCLK Output Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	$t_{OUT50\_PER}$	40.0 - 50ppm	40.0	40.0 + 50ppm	ns	–
REFCLK Clock High	$t_{OUT50\_HI}$	14	20.0	26	ns	–
REFCLK Clock Low	$t_{OUT50\_LO}$	14	20.0	26	ns	–
REFCLK Clock Rise Time, $V_{OL}$ (max) to $V_{OH}$ (min.)	$t_{OUT50\_RISE}$	–	–	2	ns	–
REFCLK Clock Fall Time, $V_{OH}$ (min.) to $V_{OL}$ (max)	$t_{OUT50\_FALL}$	–	–	2	ns	–
REFCLK Clock Jittering (p-p)	$t_{OUT50\_JIT}$	–	0.15	–	ns	–



### 5.3.10 Reduce MII Timing

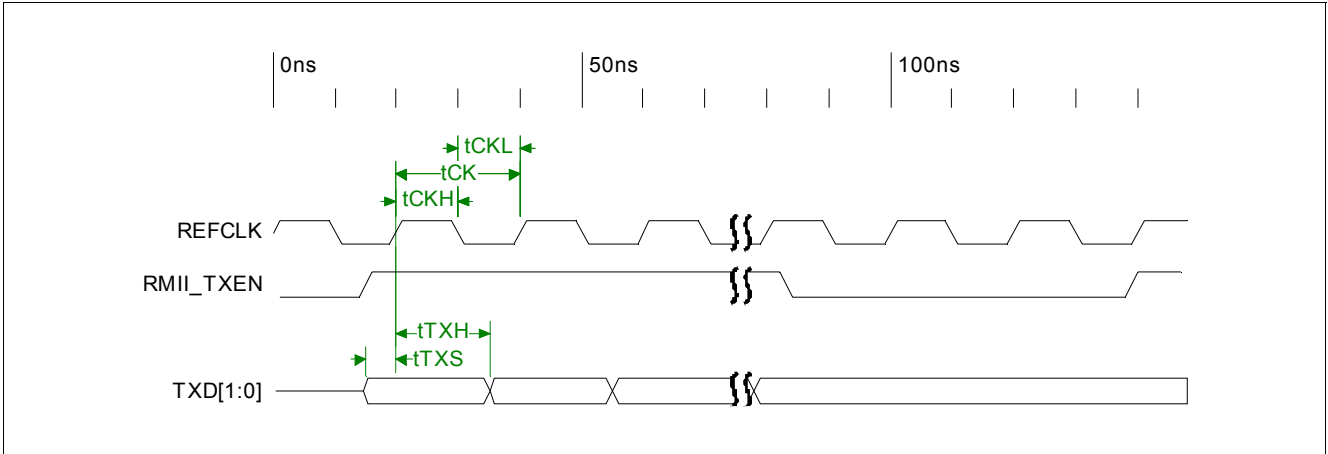


Figure 28 Reduce MII Timing (1 of 2)

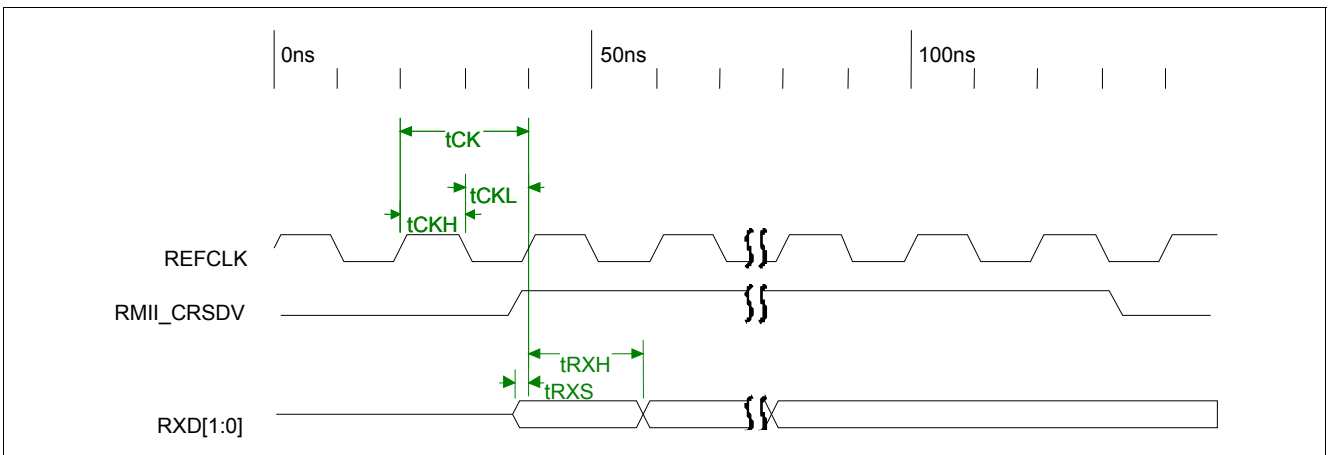


Figure 29 Reduce MII Timing (2 of 2)

Table 88 Reduce MII Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMII_REFCLK Period	$t_{CK}$	–	20	–	ns	–
RMII_REFCLK Low Period	$t_{CKL}$	–	10	–	ns	–
RMII_REFCLK High Period	$t_{CKH}$	–	10	–	ns	–
TXEN, TXD to REFCLK rising setup time	$t_{TXS}$	4	–	–	ns	–
TXE, TXD to REFCLK rising hold time	$t_{TXH}$	2	–	–	ns	–
CRSDV, RXD to REFCLK rising setup time	$t_{RXS}$	4	–	–	–	–
CRSDV, RXD to REFCLK rising hold time	$t_{RXH}$	2	–	–	–	–

### 5.3.11 GPSI (7-wire) Input Timing

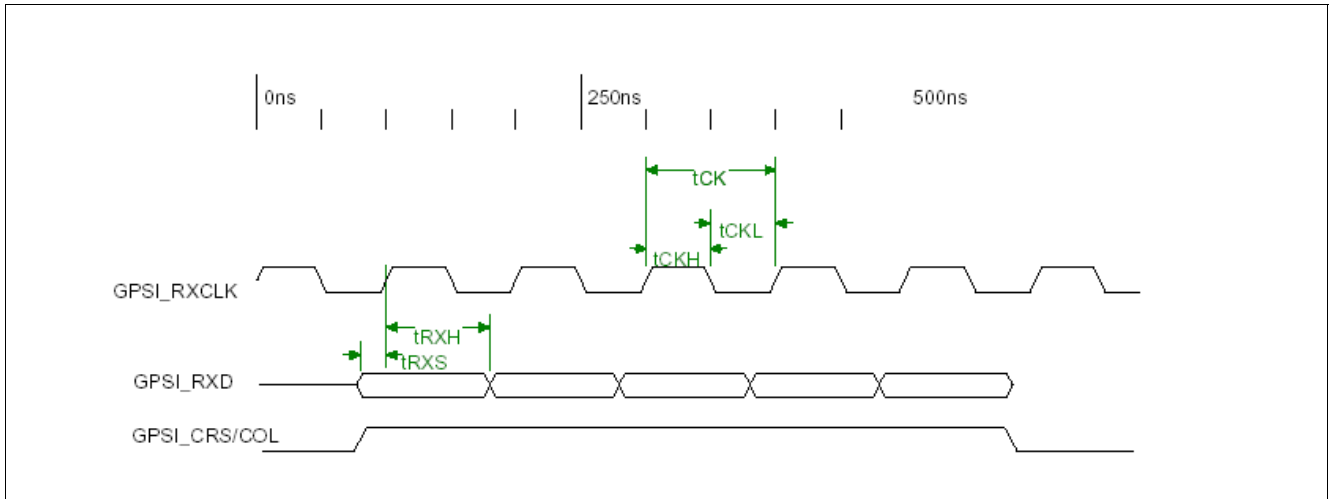


Figure 30 GPSI (7-wire) Input Timing

Table 89 GPSI (7-wire) Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_RXCLK Period	$t_{CK}$	–	100	–	ns	–
GPSI_RXCLK Low Period	$t_{CKL}$	40	–	60	ns	–
GPSI_RXCLK High Period	$t_{CKH}$	40	–	60	ns	–
GPSI_RXD, GPSI_CRD/COL to GPSI_RXCLK Rising Setup Time	$t_{RXS}$	10	–	–	ns	–
GPSI_RXD, GPSI_CRD/COL to GPSI_RXCLK Rising HoldTime	$t_{RXH}$	10	–	–	ns	–

### 5.3.12 GPSI (7-wire) Output Timing

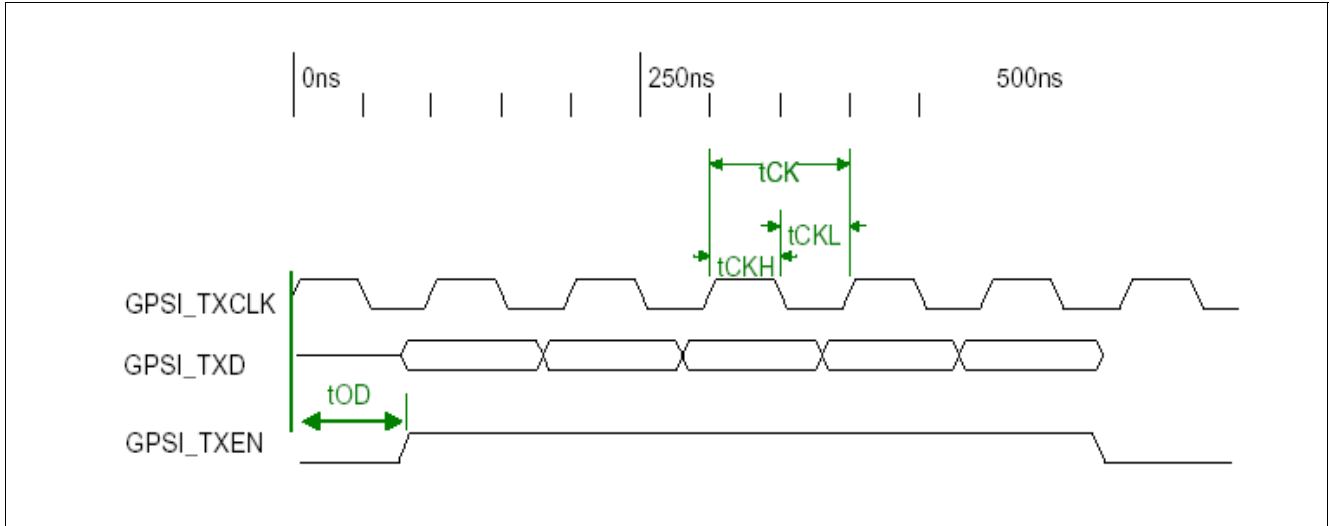


Figure 31 GPSI (7-wire) Output Timing

Table 90 GPSI (7-wire) Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
GPSI_TXCLK Period	$t_{CK}$	–	100	–	ns	–
GPSI_TXCLK Low Period	$t_{CKL}$	40	–	60	ns	–
GPSI_TXCLK High Period	$t_{CKH}$	40	–	60	ns	–
GPSI_TXCLK Rising to GPSI_TXEN/GPSI_TXD Output Delay	$t_{OD}$	50	–	70	ns	–

### 5.3.13 SDC/SDIO Timing

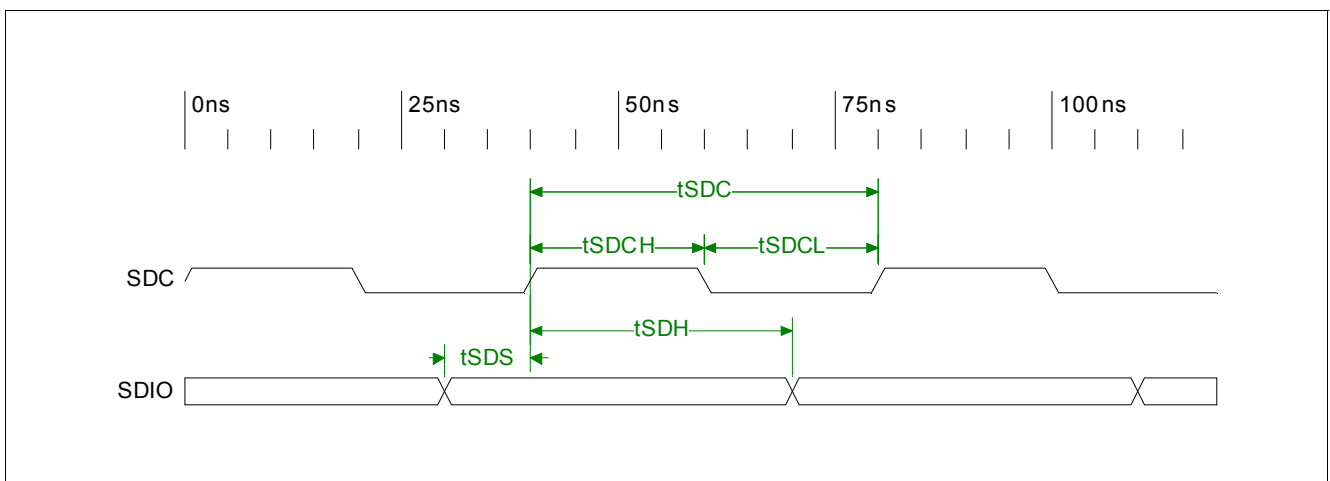
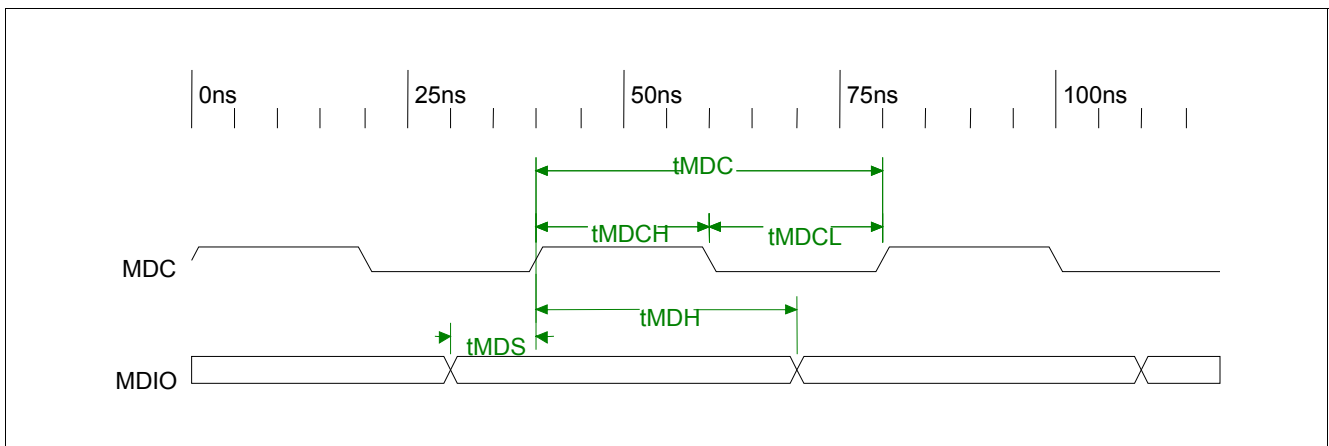


Figure 32 SDC/SDIO Timing

**Table 91 SDC/SDIO Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SDC Period	$t_{CK}$	20	–	–	ns	–
SDC Low Period	$t_{CKL}$	10	–	–	ns	–
SDC High Period	$t_{CKH}$	10	–	–	ns	–
SDIO to SDC rising setup time on read/write cycle	$t_{SDS}$	4	–	–	ns	–
SDIO to SDC rising hold time on read/write cycle	$t_{SDH}$	2	–	–	ns	–

### 5.3.14 MDC/MDIO Timing



**Figure 33 MDC/MDIO Timing**

**Table 92 MDC/MDIO Timing**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC Period	$t_{MDC}$	100	–	–	ns	–
MDC Low Period	$t_{MDCL}$	40	–	–	ns	–
MDC High Period	$t_{MDCH}$	40	–	–	ns	–
MDIO to MDC rising setup time on read/write cycle	$t_{MDS}$	–	–	10	ns	–
MDIO to MDC rising hold time on read/write cycle	$t_{MDH}$	10	–	–	ns	–

## 6 Package Outlines

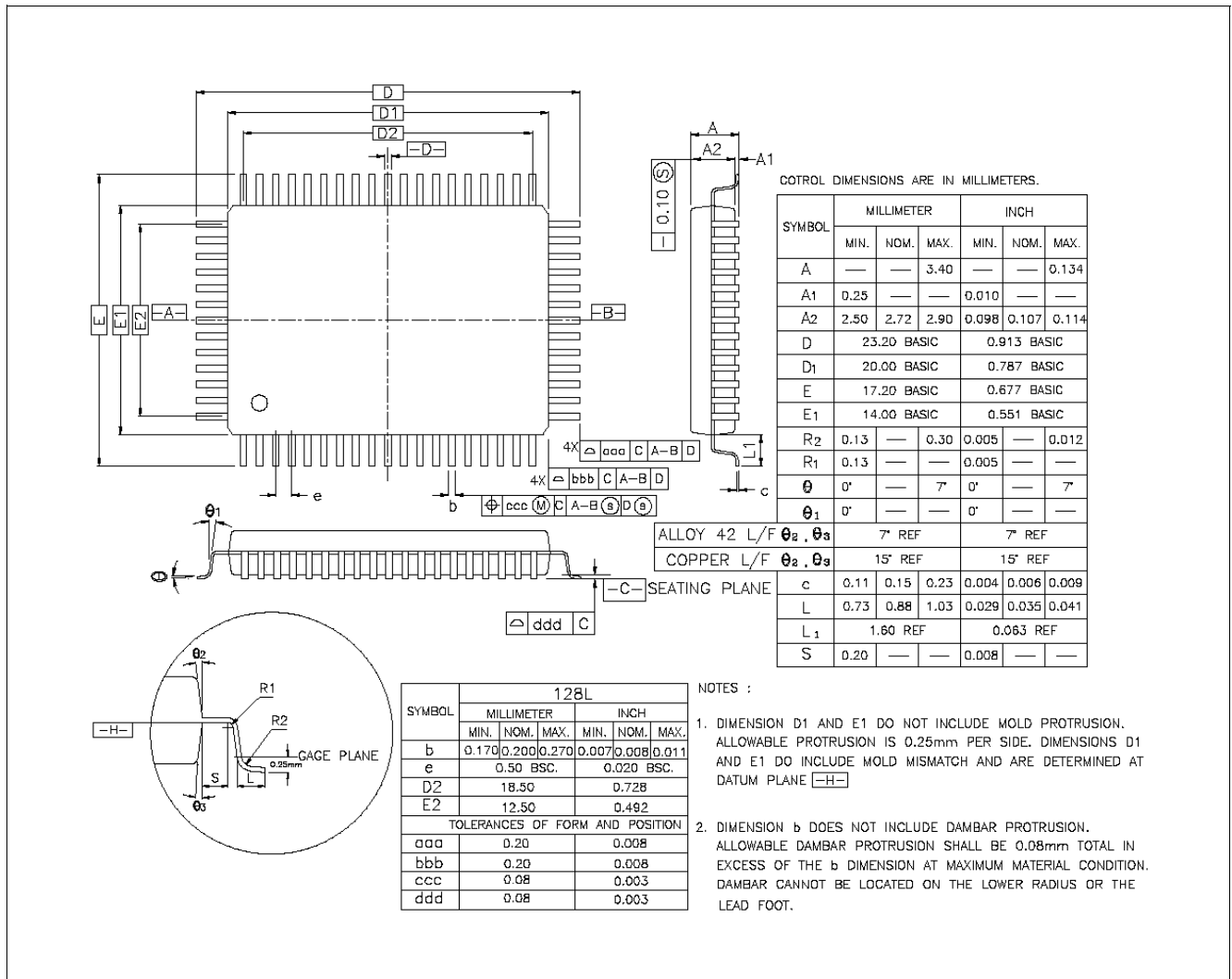


Figure 34 P-PQFP-128 Outside Dimension

### 6.1 Package Information

Product Name	Product Type	Package
6-Port 10/100 Mbit/s Single Chip Ethernet Switch Controller	Samurai-6M/MX, ADM6996M/MX-AD-T-1, Version AD	P-PQFP-128

## Terminology

### B

BER Bit Error Rate

### C

CFI Canonical Format Indicator

COL Collision

CRC Cyclic Redundancy Check

CRS Carrier Sense

CS Chip Select

### D

DA Destination Address

DI Data Input

DO Data Output

### E

EDI EEPROM Data Input

EDO EEPROM Data Output

EECS EEPROM Chip Select

EESK EEPROM Clock

ESD End of Stream Delimiter

### F

FEFI Far End Fault Indication

FET Field Effect Transistor

FLP Fast Link Pulse

### G

GND Ground

GPSI General Purpose Serial Interface

### I

IPG Inter-Packet Gap

### L

LF SR Linear Feedback Shift Register

### M

MAC Media Access Controller

MDIX MDI Crossover

MII Media Independent Interface

### N

NRZI Non Return to Zero Inverter

NRZ Non Return to Zero

### P

PCS Physical Coding Sub-layer

PHY Physical Layer

PLL Phase Lock Loop

PMA Physical Medium Attachment

PMD	Physical Medium Dependent
<b>Q</b>	
QoS	Quality of Service
QFP	Quad Flat Package
<b>R</b>	
RST	Reset
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid
RXER	Receive Data Errors
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
<b>S</b>	
SA	Source Address
SOHO	Small Office Home Office
SSD	Start of Stream Delimiter
SQE	Signal Quality Error
<b>T</b>	
TOS	Type of Service
TP	Twisted Pair
TTL	Transistor Logic
TXCLK	Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXN	Transmission Negative
TXP	Transmission Positive

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