IS66WV51216DALL
IS66/67WV51216DBLL

8Mb LOW VOLTAGE, ULTRA LOW POWER PSEUDO CMOS STATIC RAM

AUGUST 2014

FEATURES

- High-speed access time:
  – 70ns (IS66WV51216DALL, IS66/67WV51216DBLL)
  – 55ns (IS66/67WV51216DBLL)
- CMOS low power operation
- Single power supply
  – V_{DD} = 1.7V-1.95V (IS66WV51216DALL)
  – V_{DD} = 2.5V-3.6V (IS66/67WV51216DBLL)
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available
- Lead-free available

DESCRIPTION

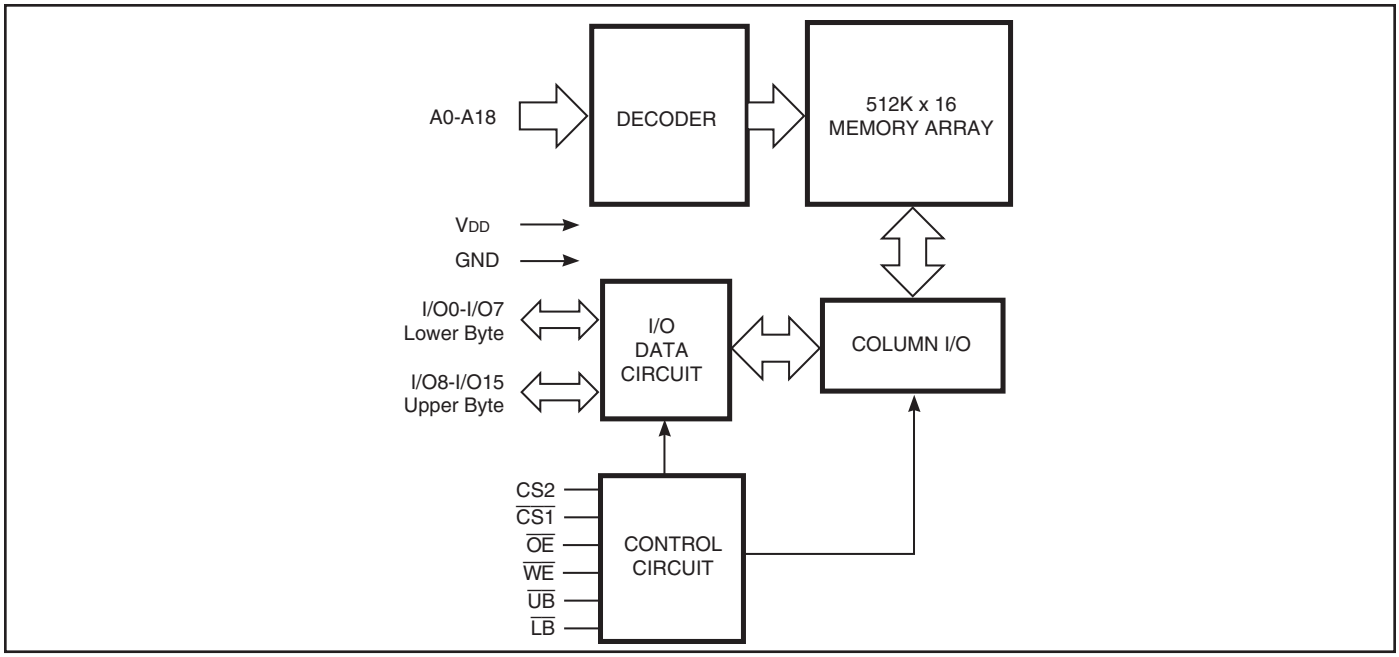
The *ISSI* IS66WV51216DALL and IS66/67WV51216DBLL are high-speed, 8M bit static RAMs organized as 512K words by 16 bits. It is fabricated using *ISSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields high-performance and low power consumption devices.

When $\overline{CS1}$ is HIGH (deselected) or when CS2 is LOW (deselected) or when $\overline{CS1}$ is LOW, CS2 is HIGH and both $\overline{LB}$ and $\overline{UB}$ are HIGH, the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs. The active LOW Write Enable ($\overline{WE}$) controls both writing and reading of the memory. A data byte allows Upper Byte ($\overline{UB}$) and Lower Byte ($\overline{LB}$) access.

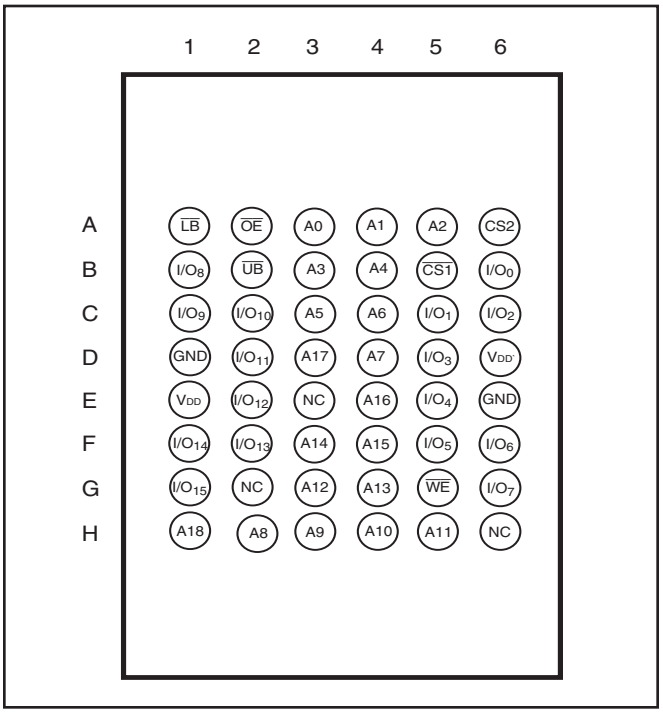
The IS66WV51216DALL and IS66/67WV51216DBLL are packaged in the JEDEC standard 48-ball mini BGA (6mm x 8mm) and 44-Pin TSOP (TYPE II). The device is aslo available for die sales.

FUNCTIONAL BLOCK DIAGRAM

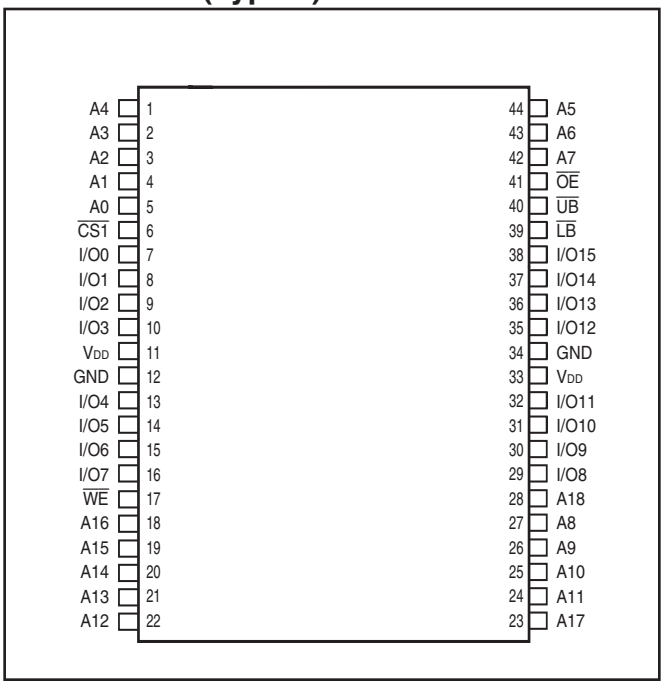


PIN CONFIGURATIONS:

48-Ball mini BGA (6mm x 8mm)



44-Pin TSOP (Type II)



PIN DESCRIPTIONS

A0-A18	Address Inputs
I/O0-I/O15	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{LB}$	Lower-byte Control (I/O0-I/O7)
$\overline{UB}$	Upper-byte Control (I/O8-I/O15)
NC	No Connection
V_{DD}	Power
GND	Ground

TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	L	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
	X	X	X	X	H	H	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	H	L	X	High-Z	High-Z	I_{CC}
	H	L	H	H	X	L	High-Z	High-Z	I_{CC}
Read	H	L	H	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	H	L	H	L	High-Z	D_{OUT}	
	H	L	H	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	H	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	H	X	H	L	High-Z	D_{IN}	
	L	L	H	X	L	L	D_{IN}	D_{IN}	

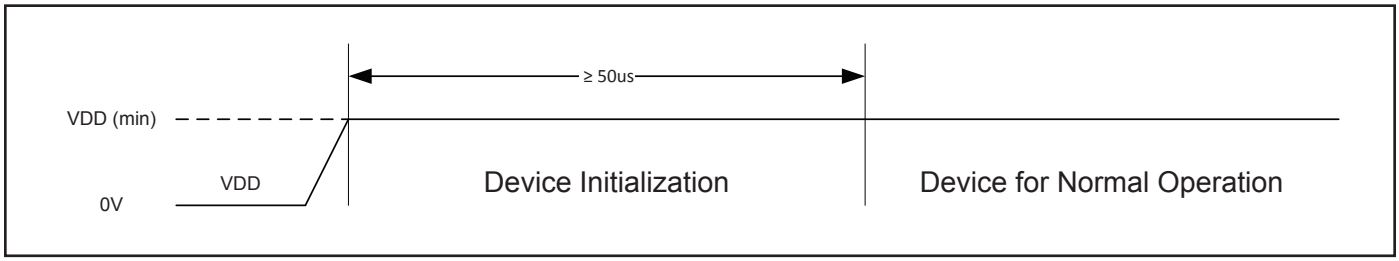
Note:
CS2 input signal pin is only available for 48-ball mini BGA package parts. CS2 input is internally enabled for 44-pin TSOP-II package parts.

OPERATING RANGE (V_{DD})

Range	Ambient Temperature	IS66WV51216DALL (70ns)	IS66WV51216DBLL (55ns, 70ns)	IS67WV51216DBLL (55ns, 70ns)
Industrial	–40°C to +85°C	1.7V - 1.95V	2.5V - 3.6V	–
Automotive, A1	–40°C to +85°C	–	–	2.5V - 3.6V
Automotive, A2	–40°C to +105°C	–	–	2.5V - 3.6V

POWER-UP INITIALIZATION

IS66WV512616DALL/DBLL and IS67WV512616DBLL include an on-chip voltage sensor used to launch the power-up initialization process. When VDD reaches a stable level at or above the VDD (min) , the device will require 50µs to complete its self-initialization process. During the initialization period, $\overline{CS}$ should remain HIGH. When initialization is complete, the device is ready for normal operation.



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.2 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
V_{DD}	V_{DD} Related to GND	–0.2 to +3.8	V
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 2.5V-3.6V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -1 mA	2.5-3.6V	2.2	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	2.5-3.6V	—	0.4	V
V_{IH}	Input HIGH Voltage[1]		2.5-3.6V	2.2	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage[1]		2.5-3.6V	–0.2	0.6	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{ILL} (min.) = –2.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max.) = V_{DD} + 2.0V AC (pulse width < 10ns). Not 100% tested.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

V_{DD} = 1.7V-1.95V

Symbol	Parameter	Test Conditions	V_{DD}	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = -0.1 mA	1.7-1.95V	1.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	1.7-1.95V	—	0.2	V
V_{IH}	Input HIGH Voltage[1]		1.7-1.95V	1.4	V_{DD} + 0.2	V
V_{IL}	Input LOW Voltage[1]		1.7-1.95V	–0.2	0.4	V
I_{LI}	Input Leakage	GND ≤ V_{IN} ≤ V_{DD}		–1	1	µA
I_{LO}	Output Leakage	GND ≤ V_{OUT} ≤ V_{DD}, Outputs Disabled		–1	1	µA

Notes:
1. V_{ILL} (min.) = –1.0V AC (pulse width < 10ns). Not 100% tested.
   V_{IHH} (max.) = V_{DD} + 1.0V AC (pulse width < 10ns). Not 100% tested.

CAPACITANCE[1]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	10	pF

Note:
1. Tested initially and after any design or process changes that may affect these parameters.

AC TEST CONDITIONS

Parameter	1.7V-1.95V (Unit)	2.5V-3.6V (Unit)
Input Pulse Level	0.4V to V_{DD}-0.2	0.4V to V_{DD}-0.3V
Input Rise and Fall Times	5 ns	5ns
Input and Output Timing and Reference Level	V_{REF}	V_{REF}
Output Load	See Figures 1 and 2	See Figures 1 and 2

	1.7V - 1.95V	2.5V - 3.6V
R1(Ω)	3070	1029
R2(Ω)	3150	1728
V_{REF}	0.9V	1.4V
V_{TM}	1.8V	2.8V

AC TEST LOADS

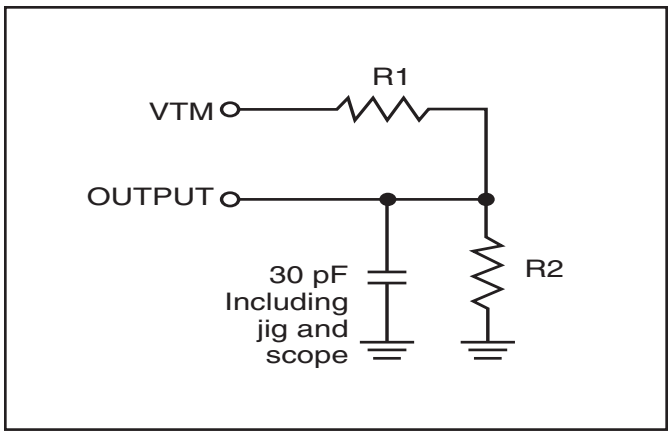


Figure 1

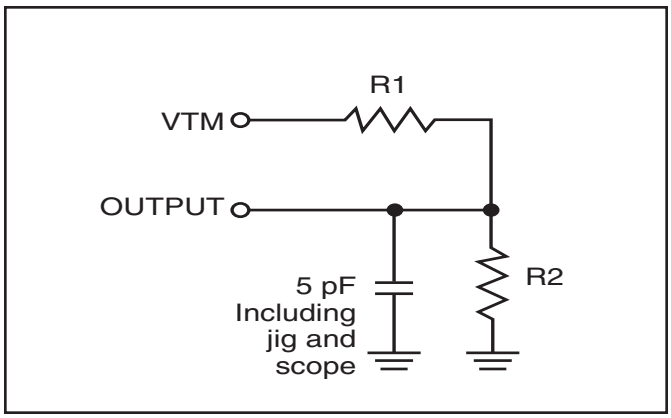


Figure 2

1.7V-1.95V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 70ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.2V	Com. Ind. Auto.	20 25 30	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V CS2 = V_{DD} – 0.2V, f = 1MHz	Com. Ind. Auto.	4 4 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com. Ind. Auto.	0.6 0.6 1	mA
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind. Auto.	100 120 150	µA
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:.
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

2.5V-3.6V POWER SUPPLY CHARACTERISTICS (Over Operating Range)

Symbol	Parameter	Test Conditions		Max. 55ns	Unit
I_{CC}	V_{DD} Dynamic Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} All Inputs 0.4V or V_{DD} – 0.3V	Com. Ind. Auto. typ.(2)	25 28 35 15	mA
I_{CC1}	Operating Supply Current	V_{DD} = Max., $\overline{CS1}$ = 0.2V $\overline{WE}$ = V_{DD} – 0.2V CS2 = V_{DD} – 0.2V, f = 1MHz	Com. Ind. Auto.	5 5 10	mA
I_{SB1}	TTL Standby Current (TTL Inputs)	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IH} , CS2 = V_{IL}, f = 1 MHz	Com. Ind. Auto.	0.6 0.6 1	mA
	OR				
	ULB Control	V_{DD} = Max., V_{IN} = V_{IH} or V_{IL} $\overline{CS1}$ = V_{IL}, f = 0, $\overline{UB}$ = V_{IH}, $\overline{LB}$ = V_{IH}			
I_{SB2}	CMOS Standby Current (CMOS Inputs)	V_{DD} = Max., $\overline{CS1}$ ≥ V_{DD} – 0.2V, CS2 ≤ 0.2V, V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0	Com. Ind. Auto. typ.(2)	100 130 150 75	µA
	OR				
	ULB Control	V_{DD} = Max., $\overline{CS1}$ = V_{IL}, CS2=V_{IH} V_{IN} ≥ V_{DD} – 0.2V, or V_{IN} ≤ 0.2V, f = 0; $\overline{UB}$ / $\overline{LB}$ = V_{DD} – 0.2V			

Note:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.
2. Typical values are measured at V_{DD} = 3.0V, T_A = 25°C and not 100% tested.

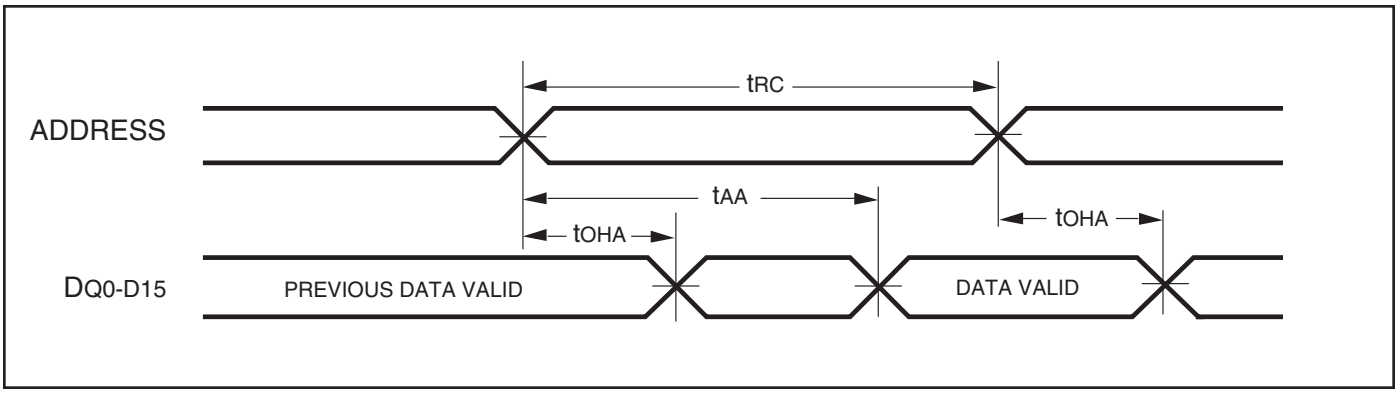
READ CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{RC}	Read Cycle Time	55	—	70	—	ns
t_{AA}	Address Access Time	—	55	—	70	ns
t_{OHA}	Output Hold Time	10	—	10	—	ns
t_{ACS1}/t_{ACS2}	$\overline{CS1}$/CS2 Access Time	—	55	—	70	ns
t_{DOE}	$\overline{OE}$ Access Time	—	25	—	35	ns
t_{HZOE}[2]	$\overline{OE}$ to High-Z Output	—	20	—	25	ns
t_{LZOE}[2]	$\overline{OE}$ to Low-Z Output	5	—	5	—	ns
t_{HZCS1}/t_{HZCS2}[2]	$\overline{CS1}$/CS2 to High-Z Output	0	20	0	25	ns
t_{LZCS1}/t_{LZCS2}[2]	$\overline{CS1}$/CS2 to Low-Z Output	10	—	10	—	ns
t_{BA}	$\overline{LB}$, $\overline{UB}$ Access Time	—	55	—	70	ns
t_{HZB}	$\overline{LB}$, $\overline{UB}$ to High-Z Output	0	20	0	25	ns
t_{LZB}	$\overline{LB}$, $\overline{UB}$ to Low-Z Output	0	—	0	—	ns
t_{CSM} [3]	CS# low pulse width	55	15,000	70	15,000	ns

Notes:
1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.
3. Refer to Avoidable Timing and Recommendations for clear definiton.

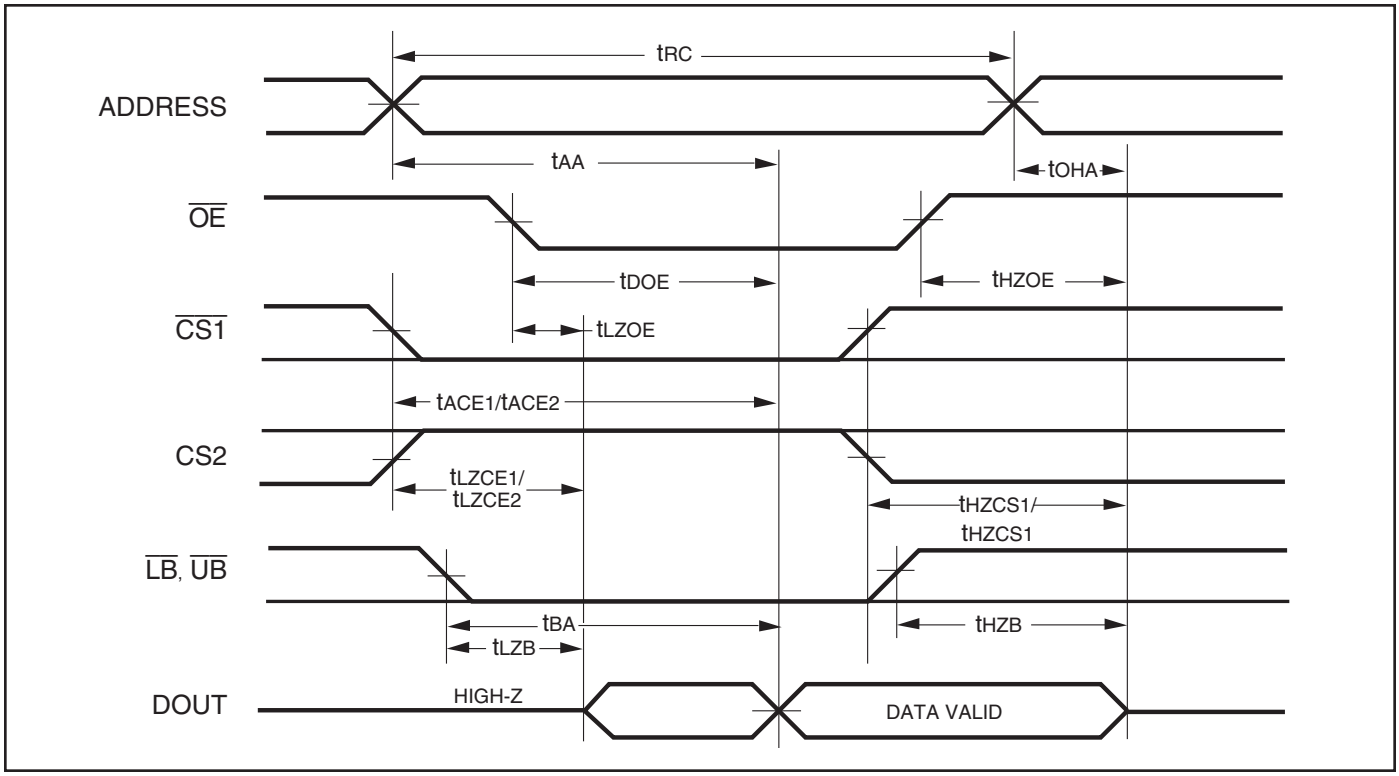
AC WAVEFORMS

READ CYCLE NO. 1[1,2] (Address Controlled) ($\overline{CS1}$ = $\overline{OE}$ = V_{IL}, CS2 = $\overline{WE}$ = V_{IH}, $\overline{UB}$ or $\overline{LB}$ = V_{IL})



AC WAVEFORMS

READ CYCLE NO. 2[1,3] ($\overline{CS1}$, CS2, $\overline{OE}$, AND $\overline{UB}$/$\overline{LB}$ Controlled)



Notes:
1. $\overline{WE}$ is HIGH for a Read Cycle.
2. The device is continuously selected. $\overline{OE}$, $\overline{CS1}$, $\overline{UB}$, or $\overline{LB}$ = V_{IL}. CS2=$\overline{WE}$=V_{IH}.
3. Address is valid prior to or coincident with $\overline{CS1}$ LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,2] (Over Operating Range)

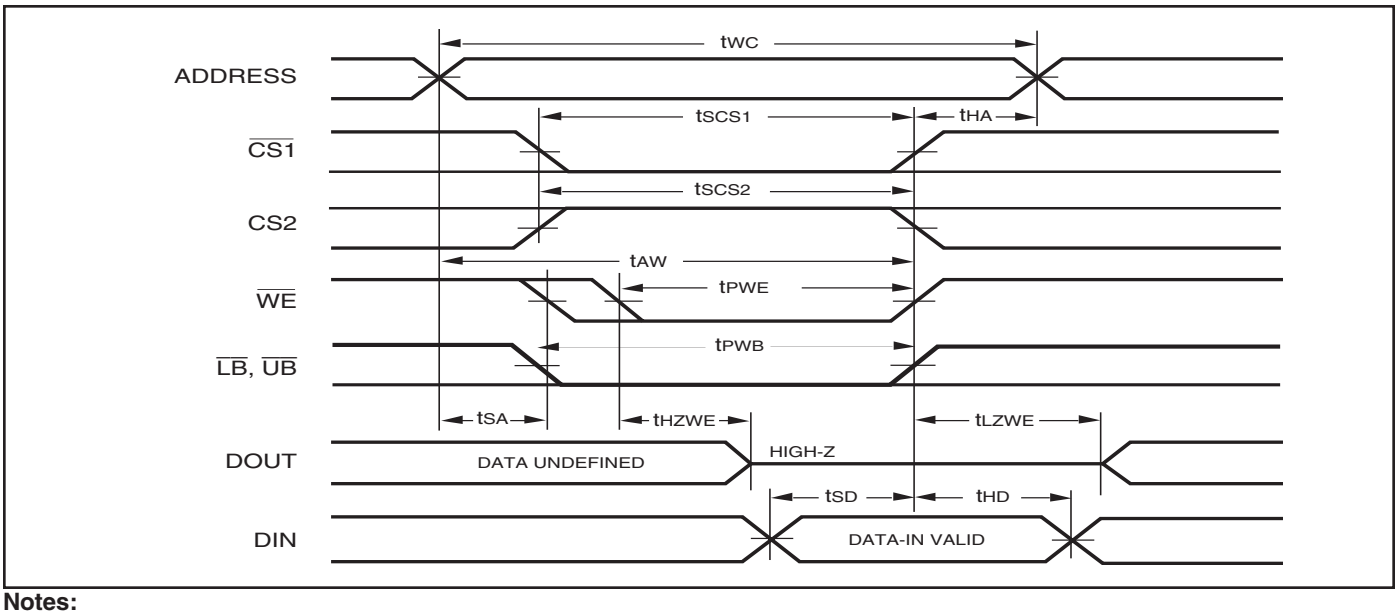
Symbol	Parameter	55 ns Min.	55 ns Max.	70 ns Min.	70 ns Max.	Unit
t_{WC}	Write Cycle Time	55	—	70	—	ns
t_{SCS1}/t_{SCS2}	$\overline{CS1}$/CS2 to Write End	45	—	60	—	ns
t_{AW}	Address Setup Time to Write End	45	—	60	—	ns
t_{HA}	Address Hold from Write End	0	—	0	—	ns
t_{SA}	Address Setup Time	0	—	0	—	ns
t_{PWB}	$\overline{LB}$, $\overline{UB}$ Valid to End of Write	45	—	60	—	ns
t_{PWE}[4]	$\overline{WE}$ Pulse Width	45	15,000[5]	60	15,000[5]	ns
t_{SD}	Data Setup to Write End	25	—	30	—	ns
t_{HD}	Data Hold from Write End	0	—	0	—	ns
t_{HZWE}[3]	$\overline{WE}$ LOW to High-Z Output	—	20	—	30	ns
t_{LZWE}[3]	$\overline{WE}$ HIGH to Low-Z Output	5	—	5	—	ns

Notes:

1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 0.9V/1.5V, input pulse levels of 0.4 to V_{DD}-0.2V/0.4V to V_{DD}-0.3V and output loading specified in Figure 1.
2. The internal write time is defined by the overlap of $\overline{CS1}$ LOW, CS2 HIGH and $\overline{UB}$ or $\overline{LB}$, and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
3. Tested with the load in Figure 2. Transition is measured ±100 mV from steady-state voltage. Not 100% tested.
4. $t_{PWE} > t_{HZWE} + t_{SD}$ when $\overline{OE}$ is LOW.
5. Refer to Avoidable Timing and Recommendations for clear definition.

AC WAVEFORMS

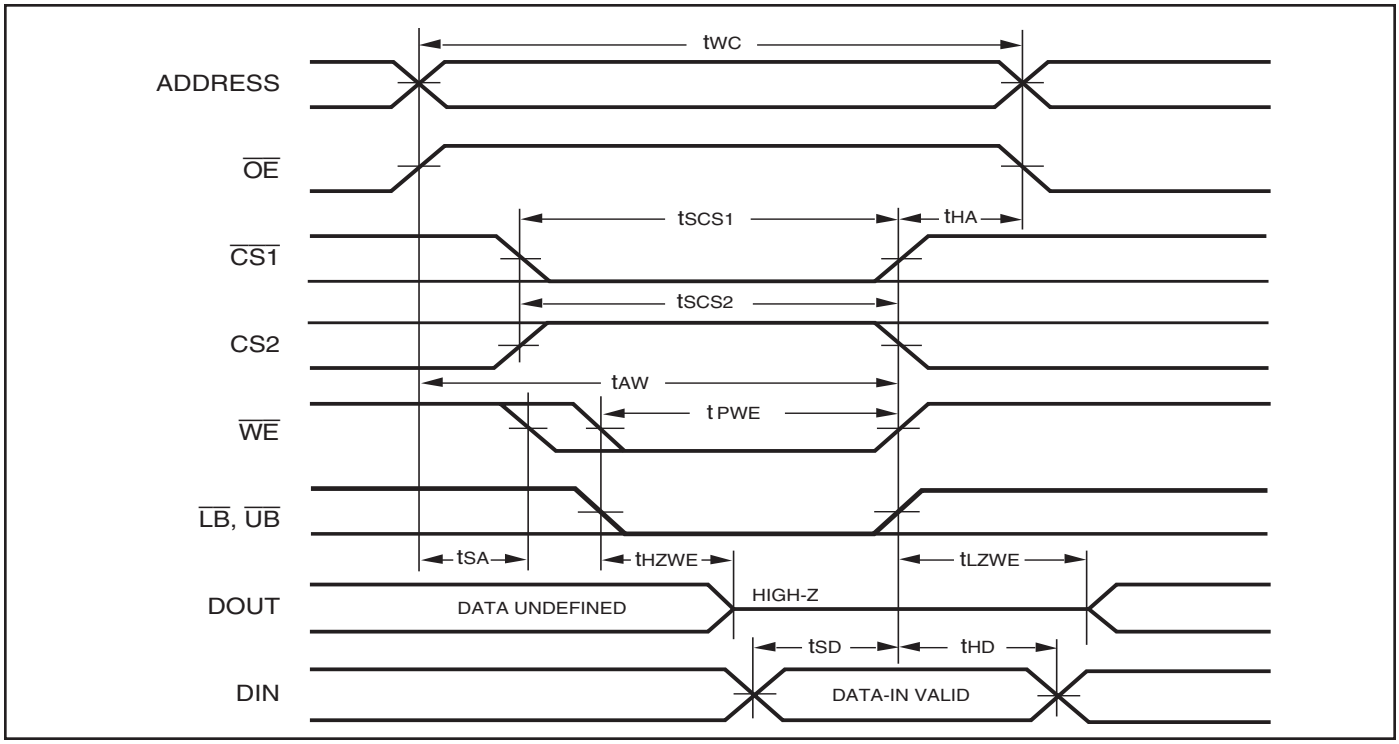
WRITE CYCLE NO. 1[1,2] ($\overline{CS1}$ Controlled, $\overline{OE}$ = HIGH or LOW)



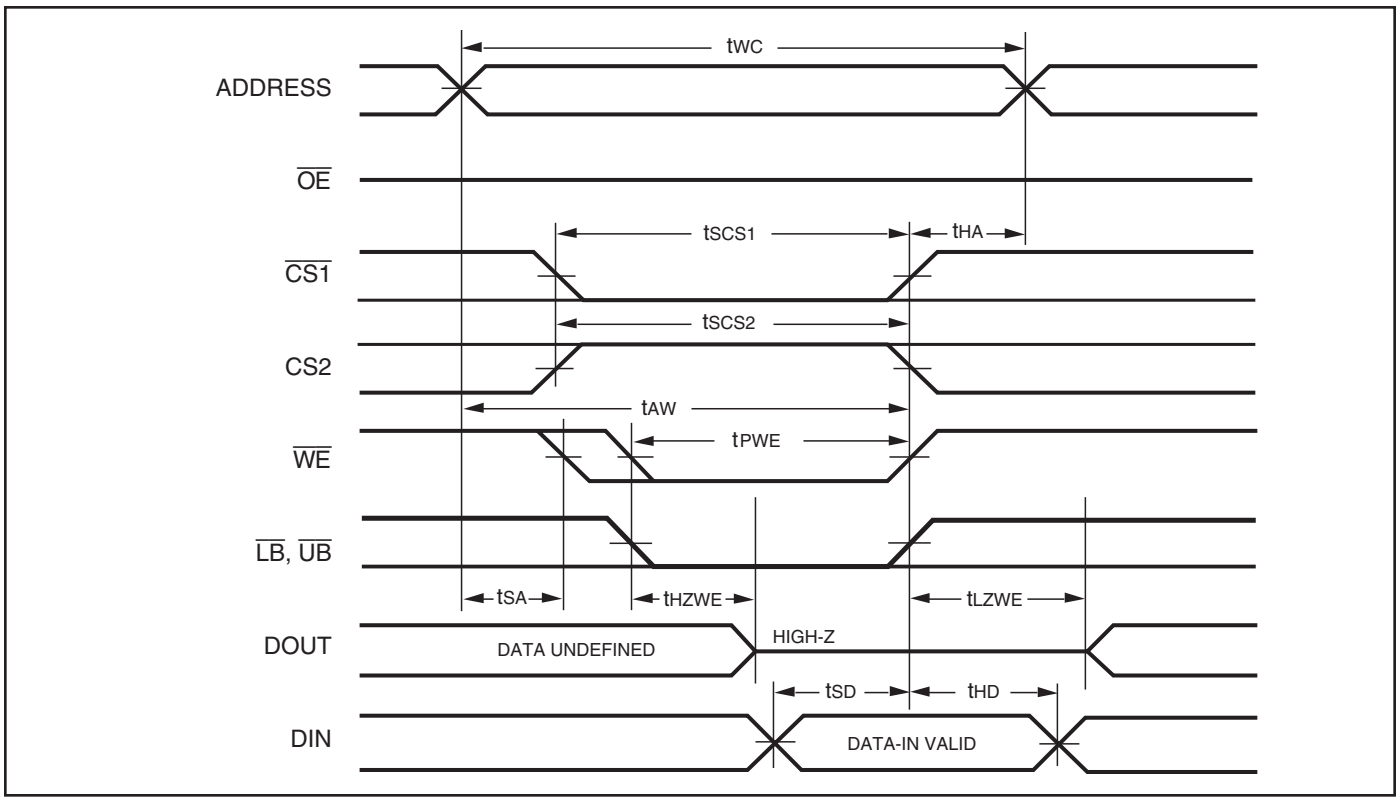
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the $\overline{CS1}$, CS2 and $\overline{WE}$ inputs and at least one of the $\overline{LB}$ and $\overline{UB}$ inputs being in the LOW state.
2. WRITE = ($\overline{CS1}$) [($\overline{LB}$) = ($\overline{UB}$)] ($\overline{WE}$).

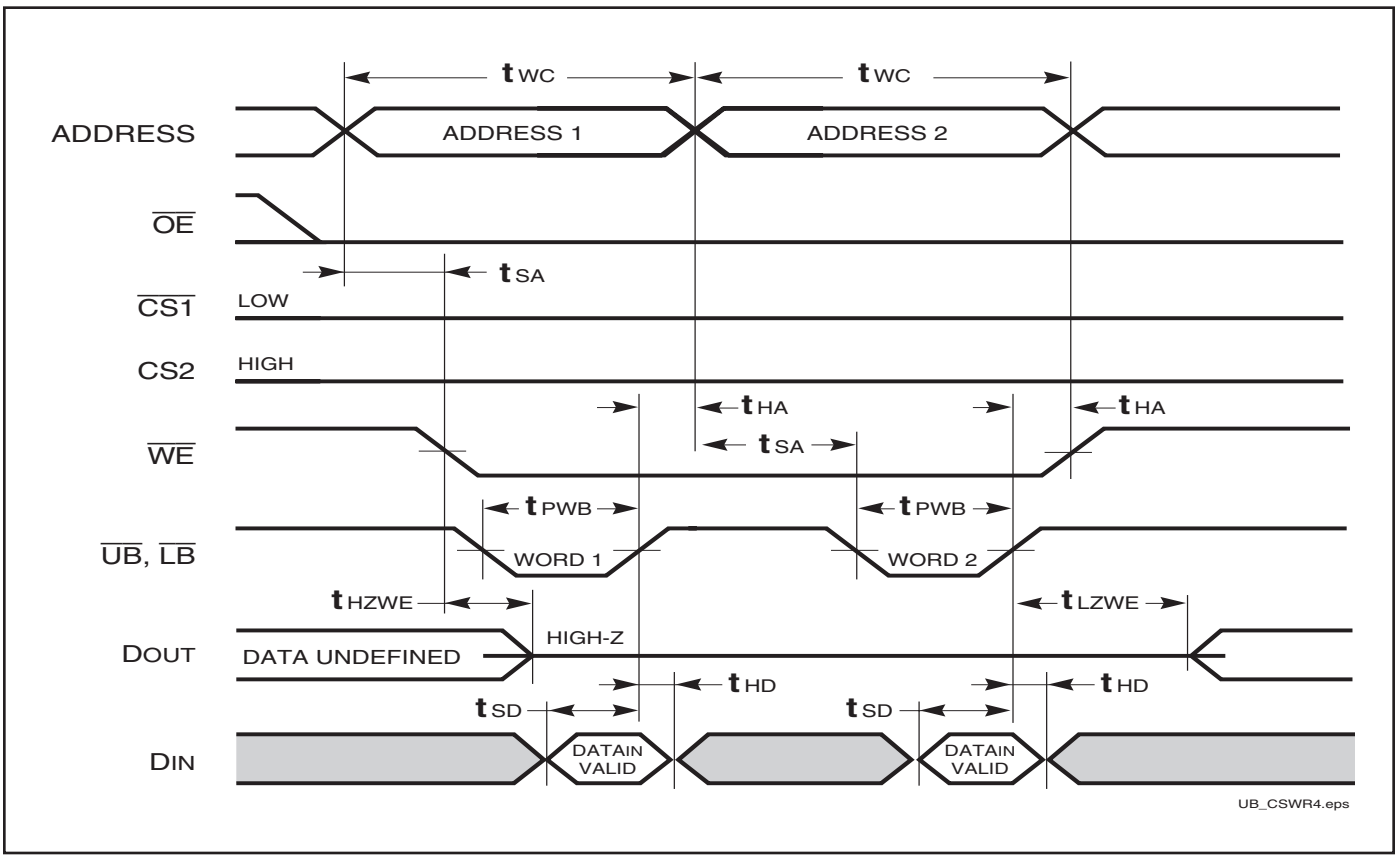
WRITE CYCLE NO. 2 ($\overline{WE}$ Controlled: $\overline{OE}$ is HIGH During Write Cycle)



WRITE CYCLE NO. 3 ($\overline{WE}$ Controlled: $\overline{OE}$ is LOW During Write Cycle)



WRITE CYCLE NO. 4 ($\overline{UB}$/$\overline{LB}$ Controlled)



AVOIDABLE TIMING AND RECOMMENDATIONS

Figure 2a

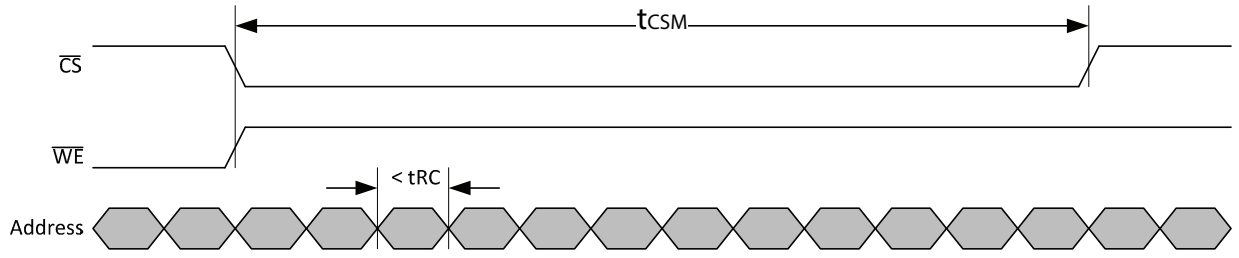


Figure 2b

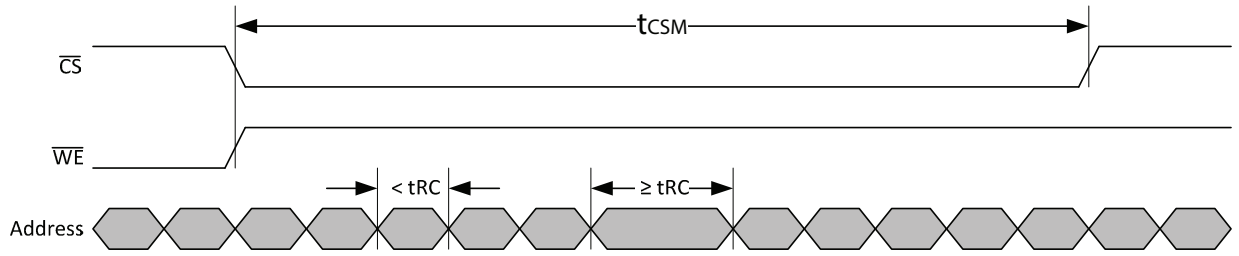


Figure 2c

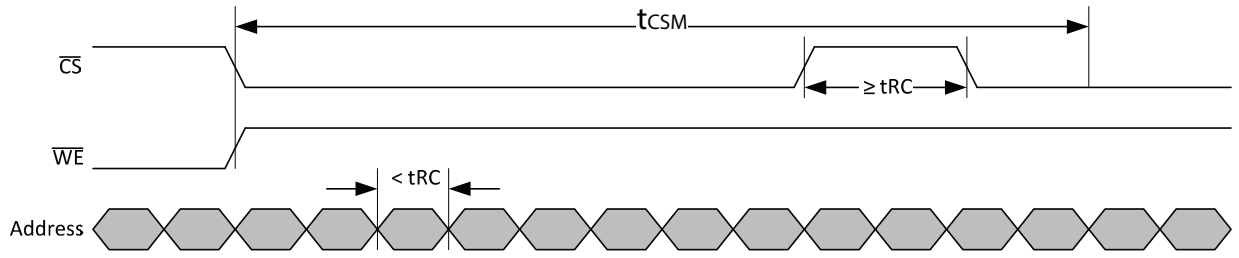
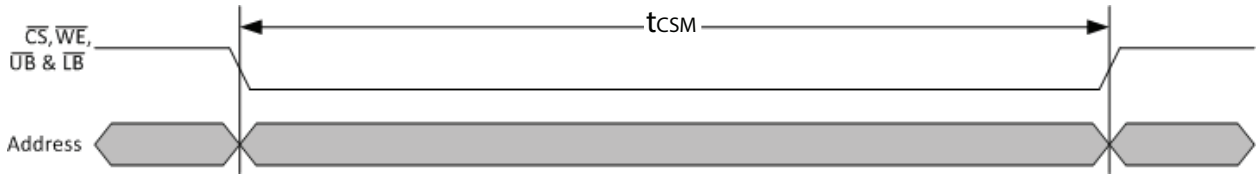


Figure 3a



AVOIDABLE TIMING AND RECOMMENDATIONS

Figure 3b

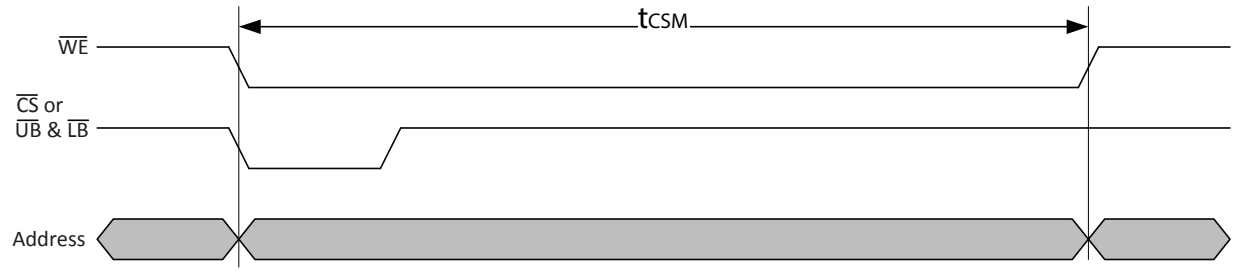
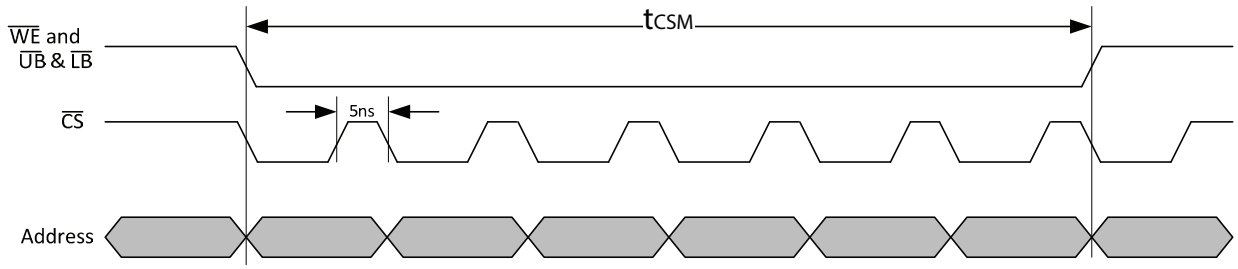


Figure 4



Notes:

1. PSRAM uses DRAM cell which needs a REFRESH action periodically to retain the information. This REFRESH action is performed internally as part of a READ cycle or when the device is not selected. A hidden REFRESH action has to be executed by the device at least once every 15µs.
2. Figure 2a shows a timing example in which consecutive READ cycles occurs in intervals less than the tRC spec while the device is selected for a period of 15µs. This timing should be avoided because output data from these READ cycles are not guaranteed to be valid due to violation of the tRC spec. This timing also prohibits the device from performing a hidden REFRESH action properly. Examples on how to avoid the timing in Figure 2a are shown in Figure 2b and 2c.
3. Figure 3a shows a timing example in which a single WRITE operation is maintained for a period greater than 15µs. Since a REFRESH action cannot be performed during a WRITE operation, information stored in the device will not be retained if this timing occurs. A WRITE operation is initiated when active LOW signals $\overline{WE}$, $\overline{CS}$, $\overline{UB}$ and $\overline{LB}$ are enabled (logic LOW) but any one of these signals can be disabled (logic HIGH) to complete the WRITE operation. Figure 3b is a timing example of using signal $\overline{CS}$ being disabled to complete the WRITE operation.
4. Since a REFRESH action cannot be performed during a WRITE operation, consecutive WRITE cycles occurring for a total period greater than 15µs are not permitted. However, executing consecutive WRITE cycles greater than 15µs is acceptable if either $\overline{WE}$, $\overline{CS}$, or both $\overline{UB}$ and $\overline{LB}$, are disabled (logic HIGH) for a period of at least 5ns or higher and can be done once or multiple times. An example using $\overline{CS}$ signal is shown in Figure 4

IS66WV51216DALL

Industrial Range: -40°C to +85°C
Voltage Range: 1.7V to 1.95V

Speed (ns)	Order Part No.	Package
70	IS66WV51216DALL-70TLI	TSOP-II, Lead-free
	IS66WV51216DALL-70BLI	mini BGA (6mm x 8mm), Lead-free

IS66WV51216DBLL

Industrial Range: -40°C to +85°C
Voltage Range: 2.5V to 3.6V

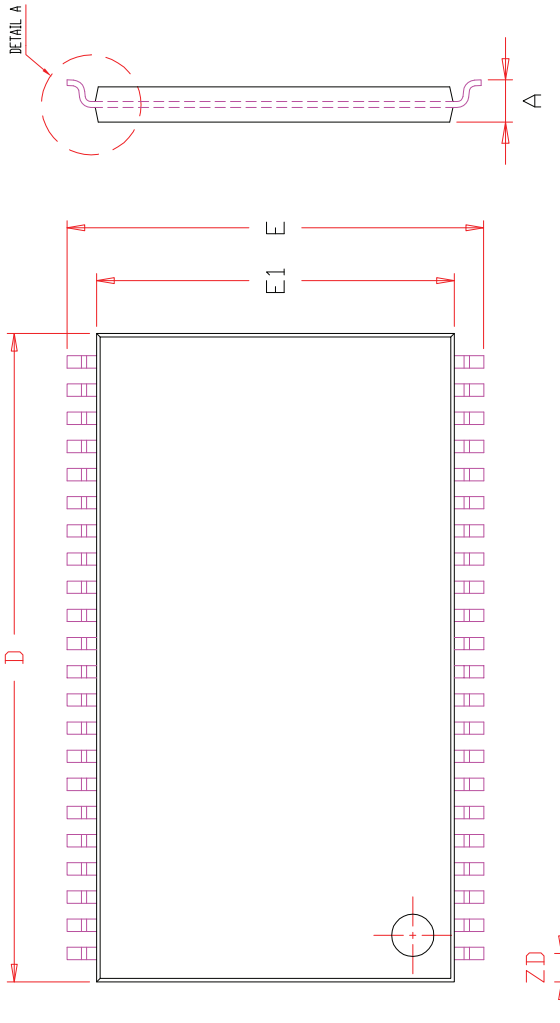
Speed (ns)	Order Part No.	Package
55	IS66WV51216DBLL-55TLI	TSOP-II, Lead-free
	T1164A-55TLI	TSOP-II, Lead-free, SPA 1164A
	IS66WV51216DBLL-55BLI	mini BGA (6mm x 8mm), Lead-free
70	IS66WV51216DBLL-70TLI	TSOP-II, Lead-free
	IS66WV51216DBLL-70BLI	mini BGA (6mm x 8mm), Lead-free

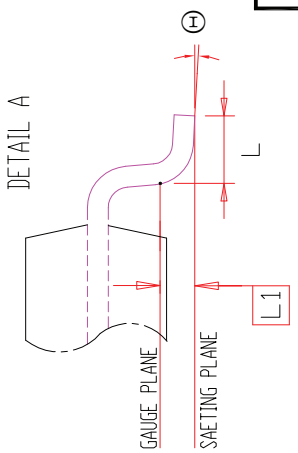
IS67WV51216DBLL

Automotive (A1) Range: -40°C to +85°C
Voltage Range: 2.5V to 3.6V

Speed (ns)	Order Part No.	Package
55	IS67WV51216DBLL-55TLA1	TSOP-II, Lead-free
	IS67WV51216DBLL-55BLA1	mini BGA (6mm x 8mm), Lead-free
70	IS67WV51216DBLL-70TLA1	TSOP-II, Lead-free
	IS67WV51216DBLL-70BLA1	mini BGA (6mm x 8mm), Lead-free

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.00	—	1.20	0.039	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	—	0.45	0.012	—	0.018
D	18.28	18.41	18.54	0.720	0.725	0.730
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
e	0.80 BSC.			0.031 BSC.		
L	0.40	—	0.69	0.016	—	0.027
L1	0.25 BSC.			0.010 BSC.		
ZD	0.805 REF.			0.032 REF.		
Θ	0	—	8°	0	—	8°





NOTE :

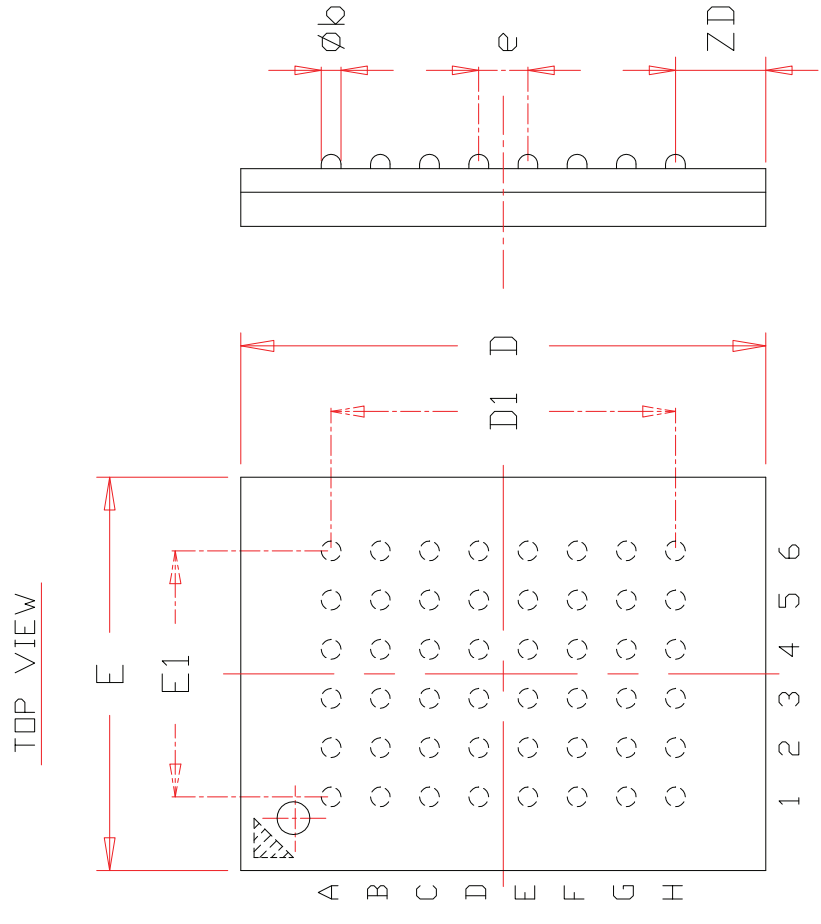
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

TITLE	44L 400mil TSOP-2 Package Outline	REV.	F	DATE	06/04/2008

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.20	—	0.30	0.008	—	0.012
øb	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	5.25 BSC			0.207 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	3.75 BSC			0.148 BSC		
e	0.75 BSC,			0.030 BSC,		
ZD	1.375 REF,			0.054 REF,		
ZE	1.125 REF,			0.044 REF,		

NOTE :

1. CONTROLLING DIMENSION : MM .
2. Reference document : JEDEC MO-207



ISSI	TITLE	48L 6x8mm TF-BGA Package Outline	REV. C DATE 08/12/2008